

Figure 1a
Prior Art

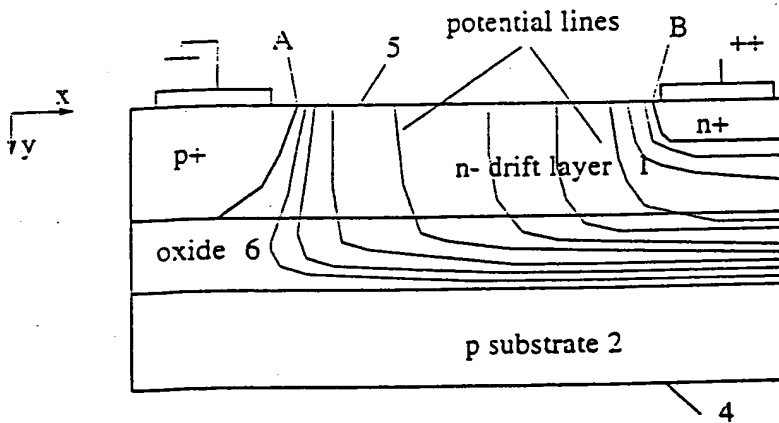
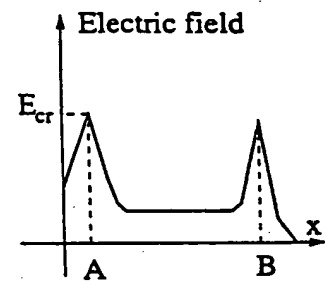
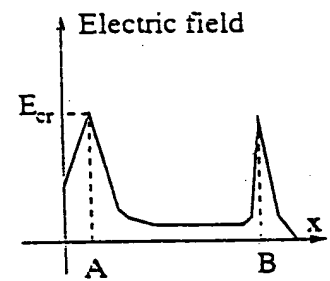


Figure 1b
Prior Art



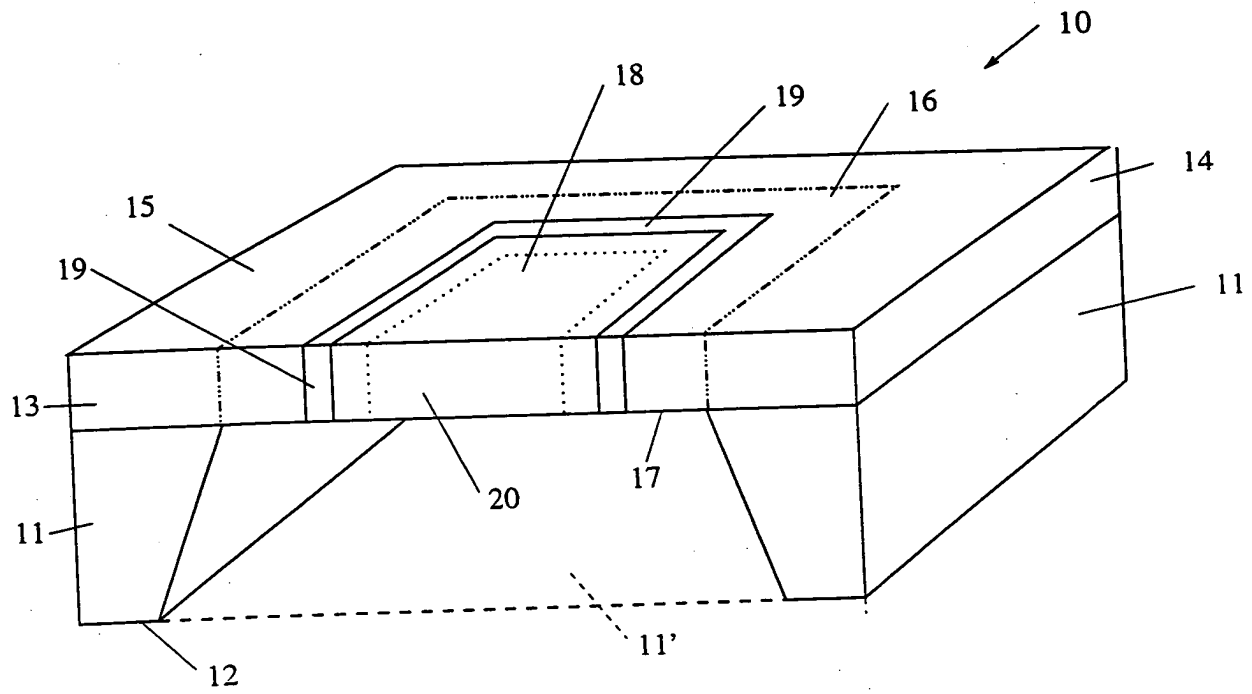


Figure 2a

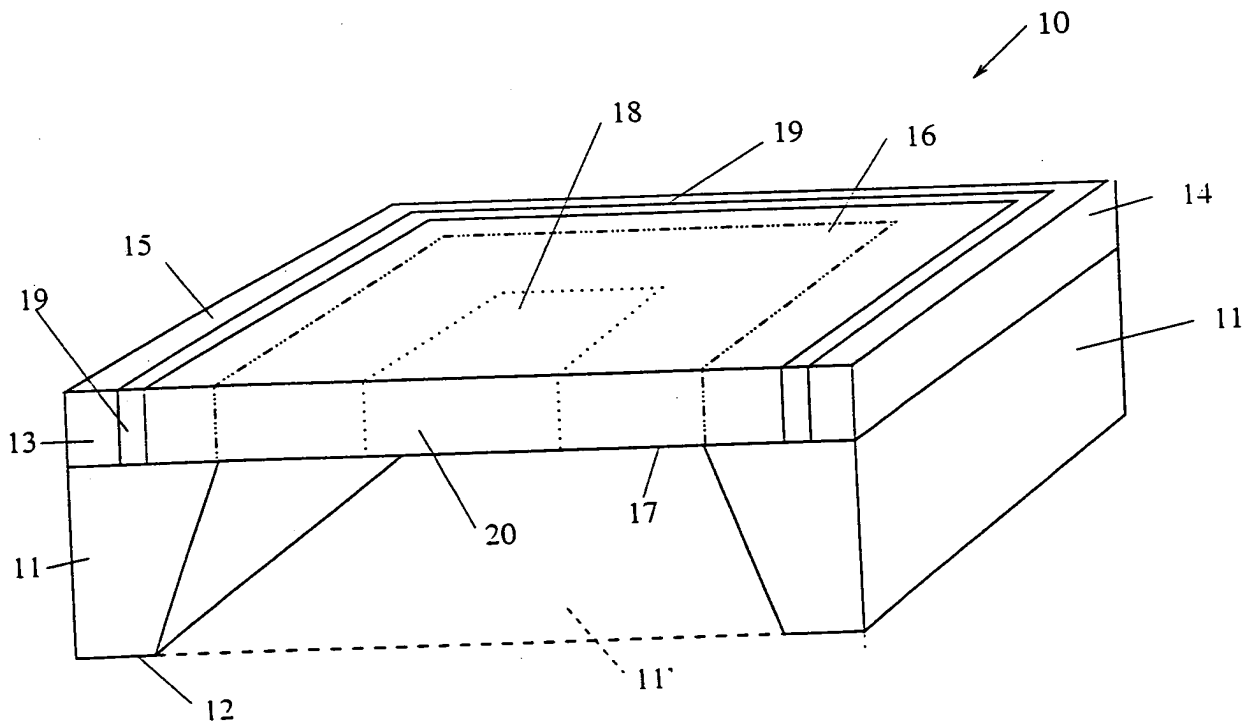


Figure 2b

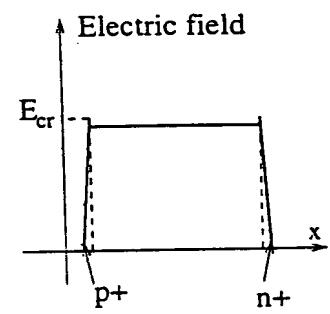


Figure 3a

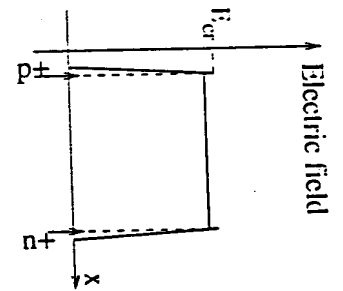


Figure 3b

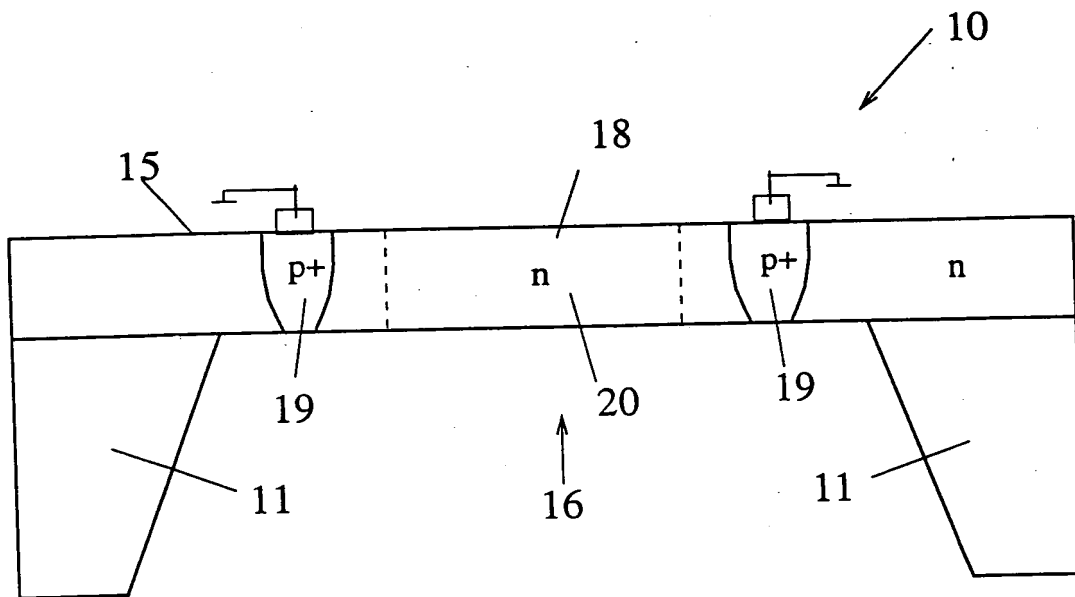


Figure 4a

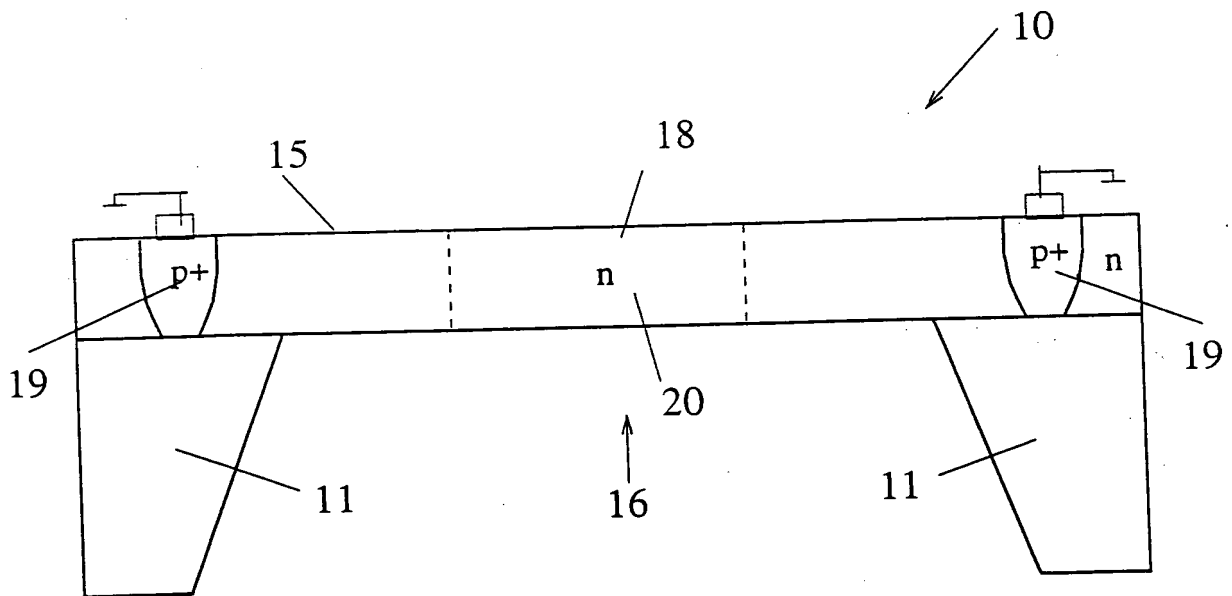


Figure 4b

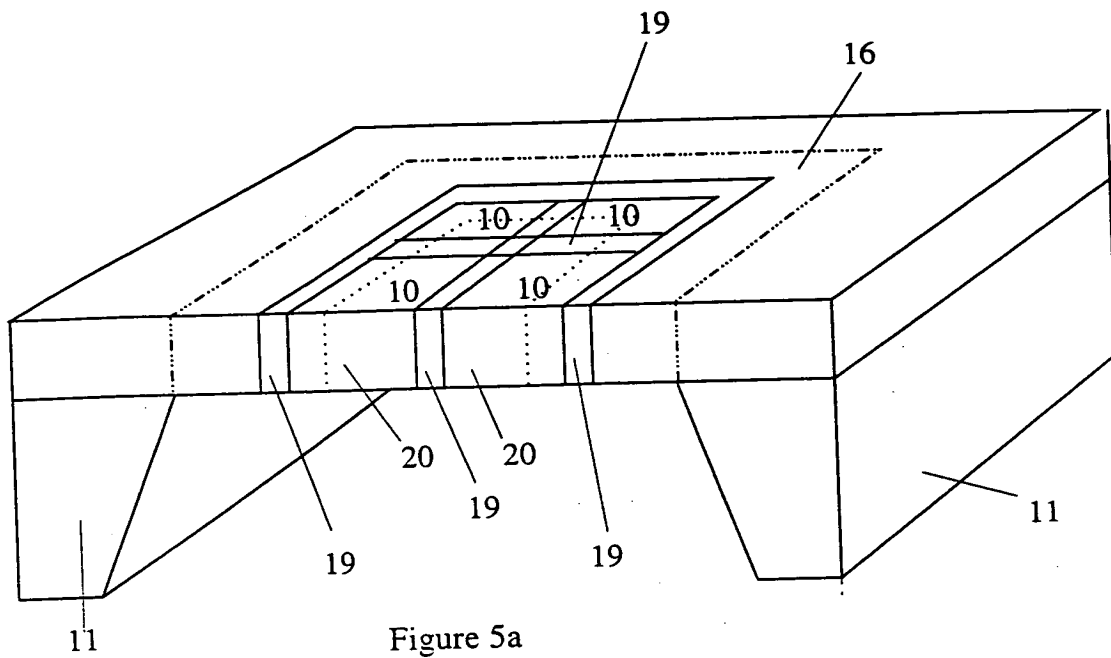


Figure 5a

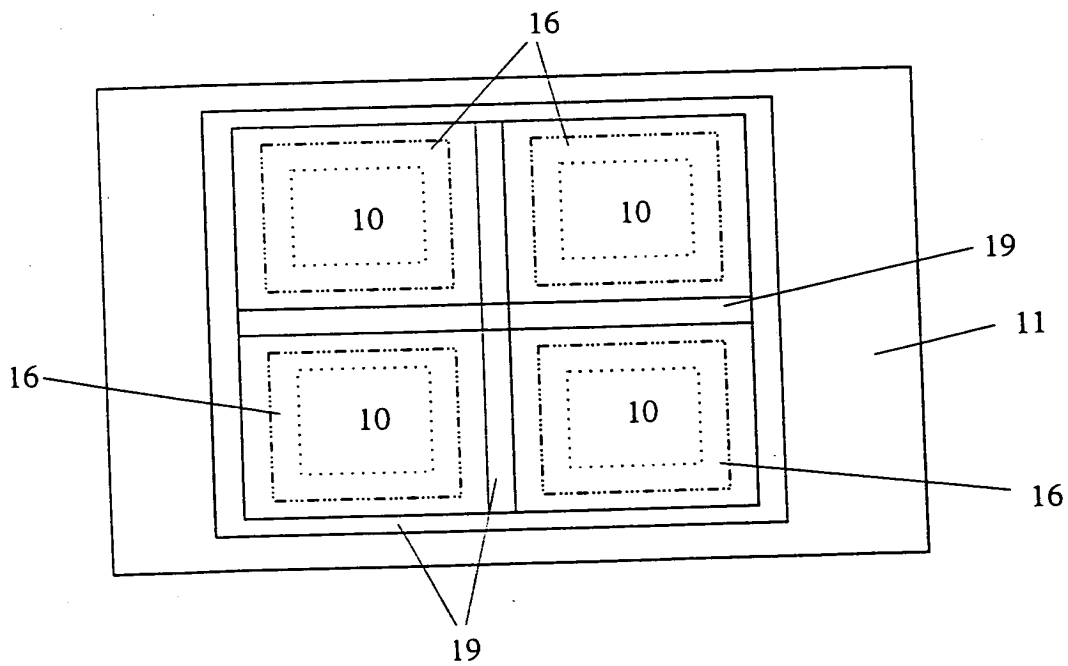


Figure 5b

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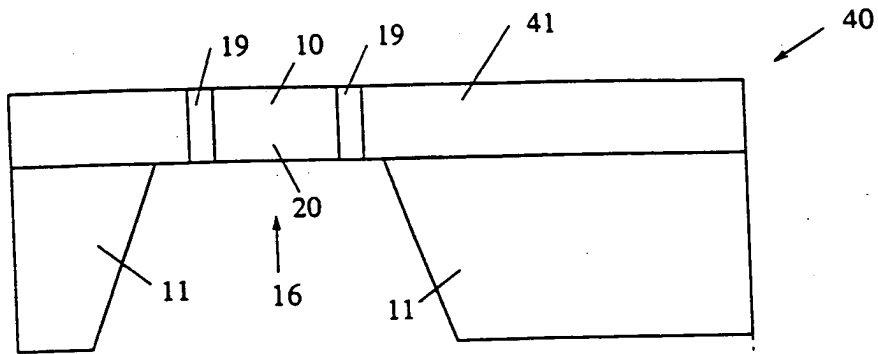


Figure 6a

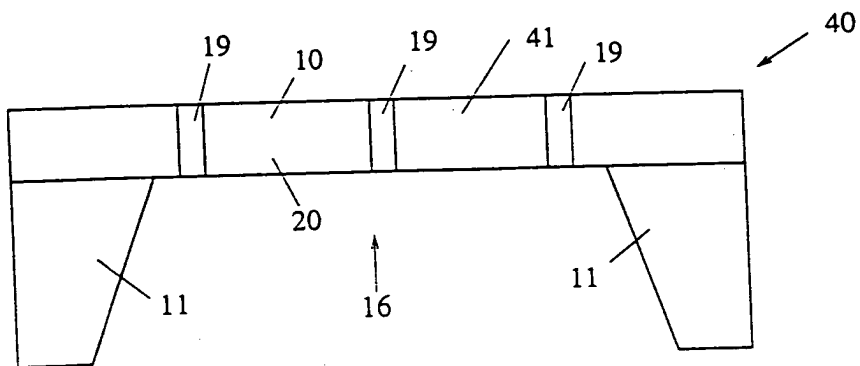


Figure 6b

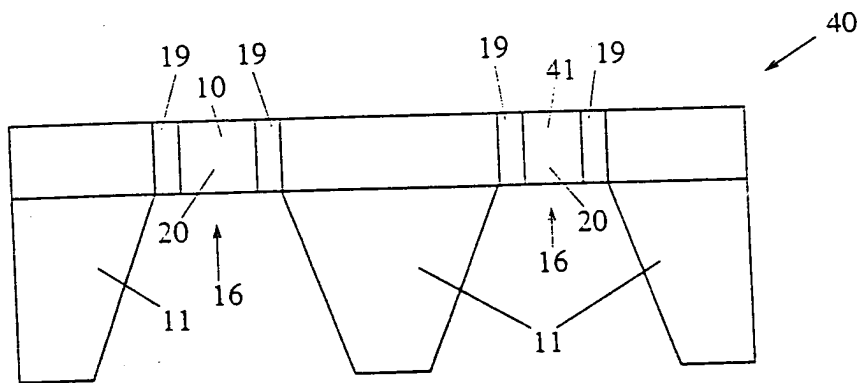


Figure 6c

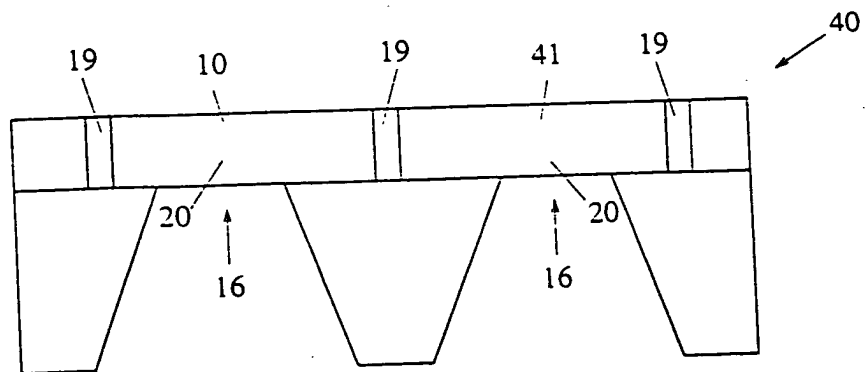


Figure 6d

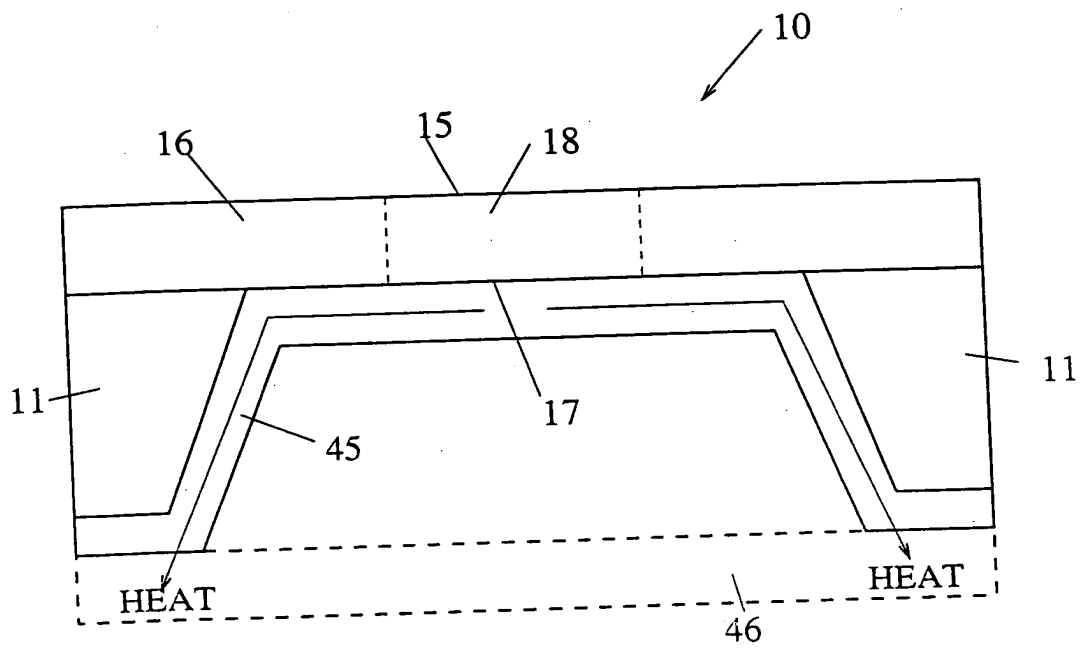


Figure 7

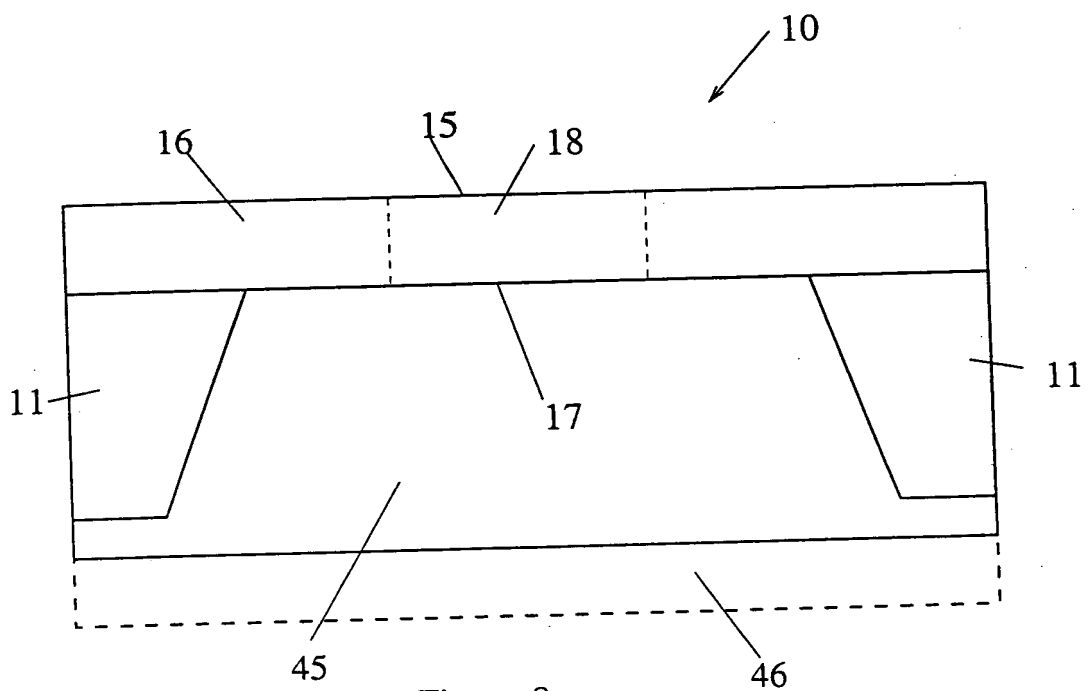


Figure 8

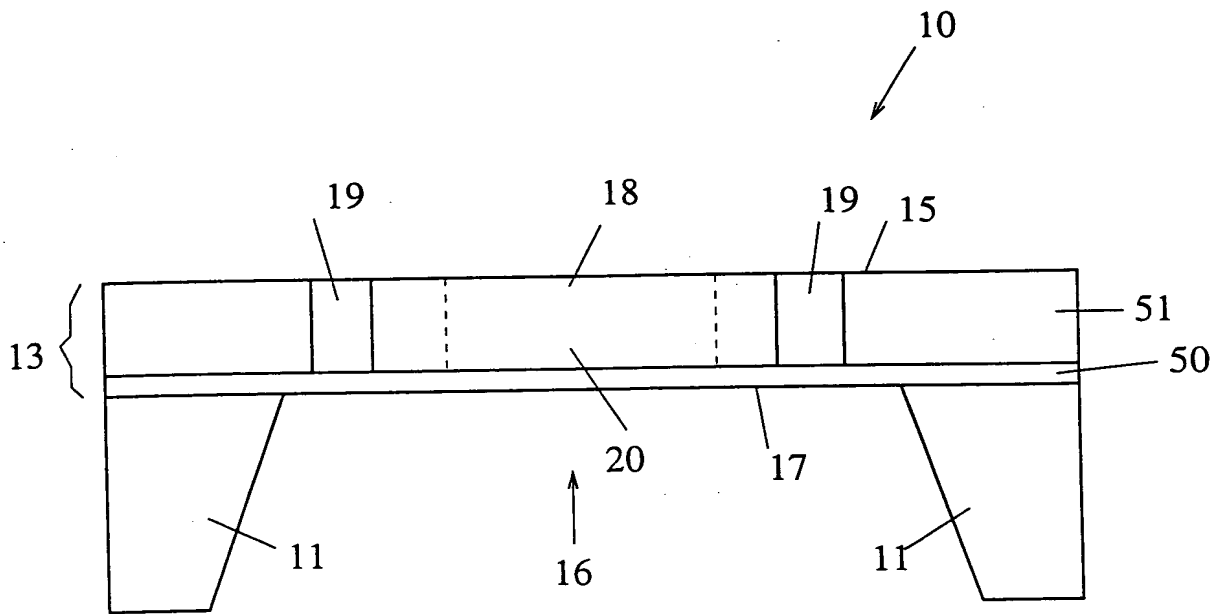


Figure 9a

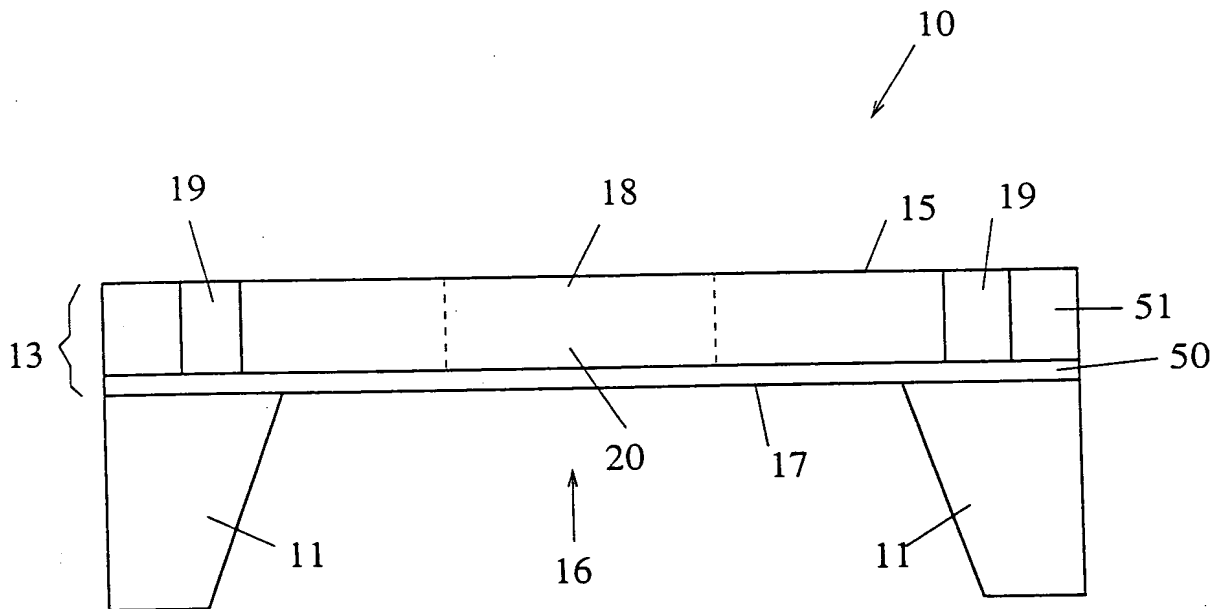


Figure 9b

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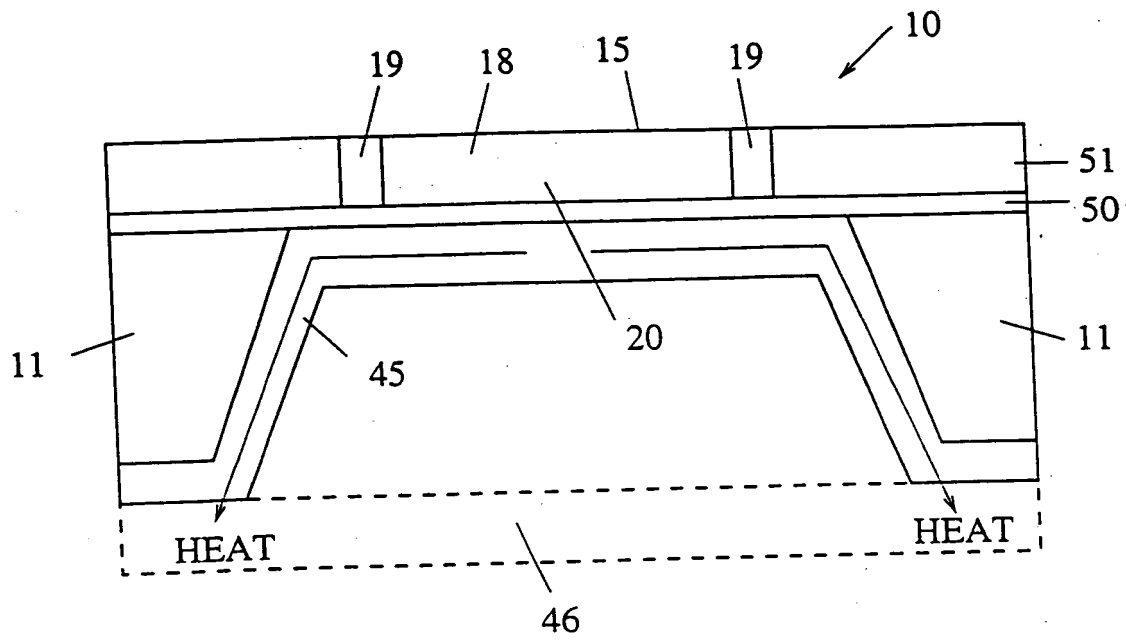


Figure 10a

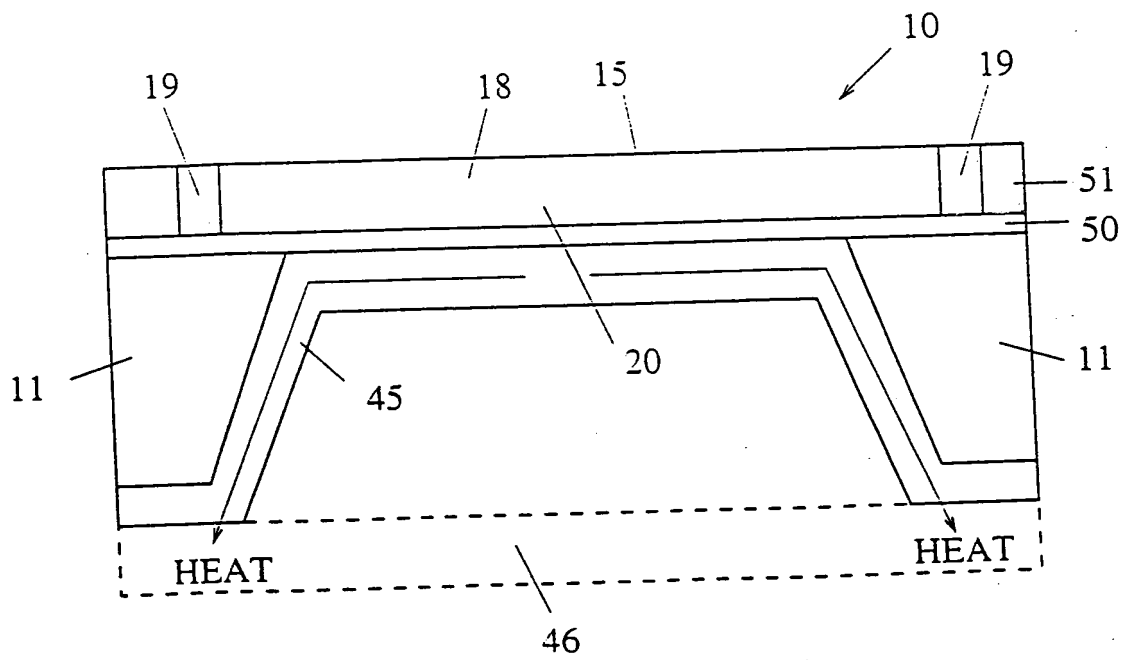


Figure 10b

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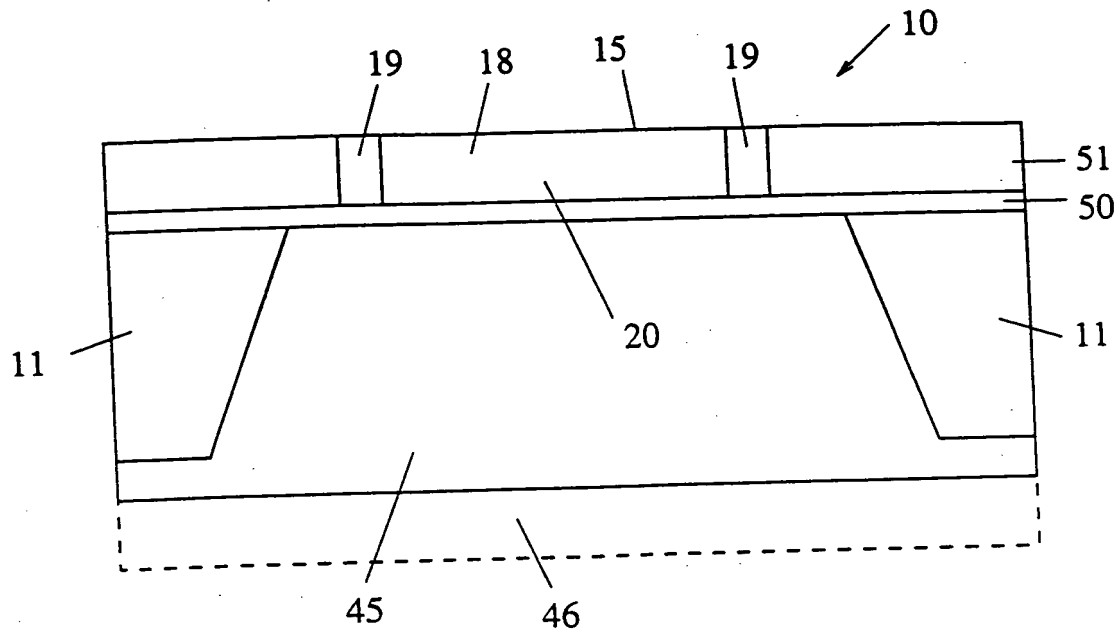


Figure 11a

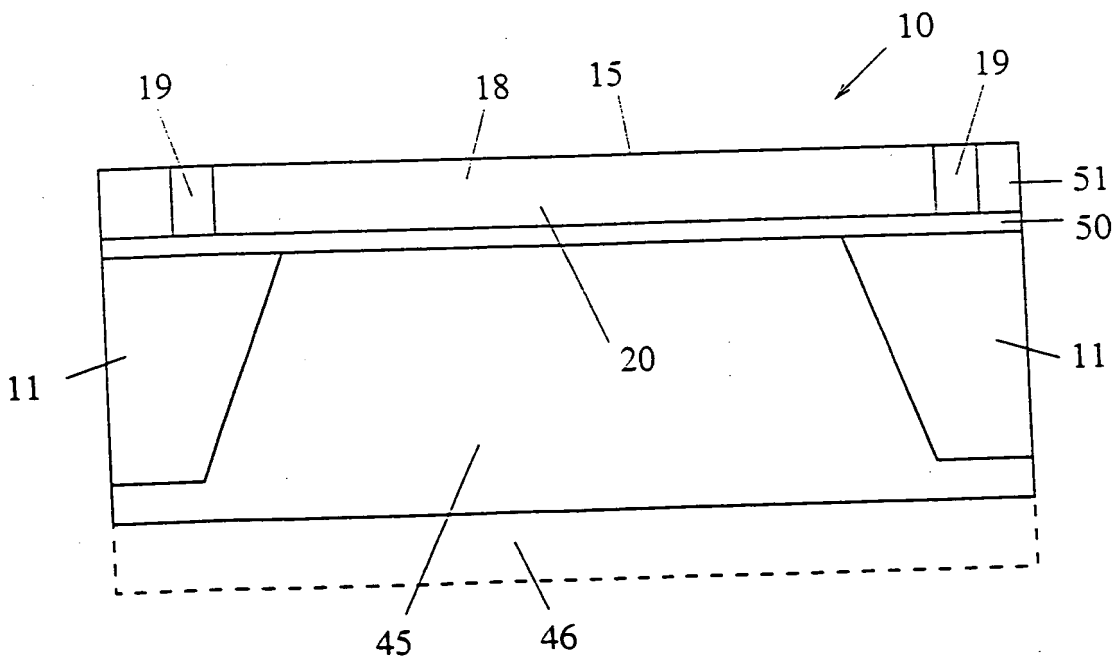


Figure 11b

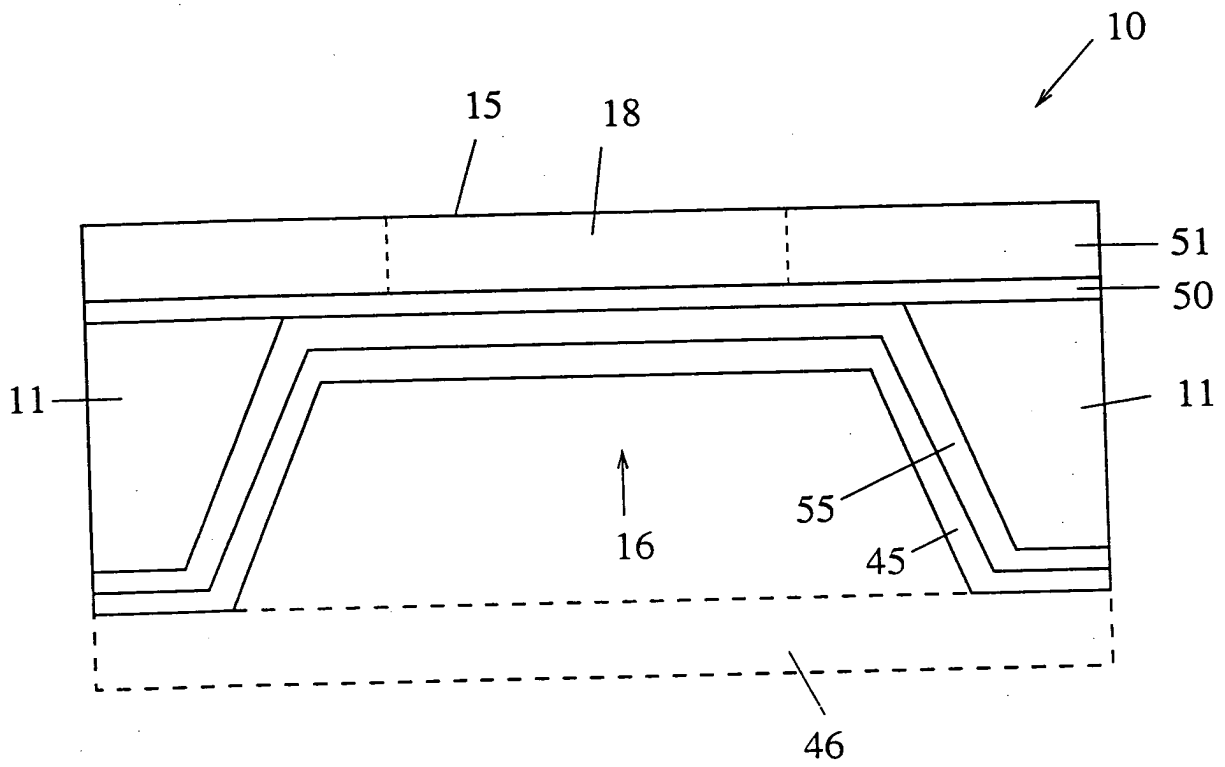


Figure 12

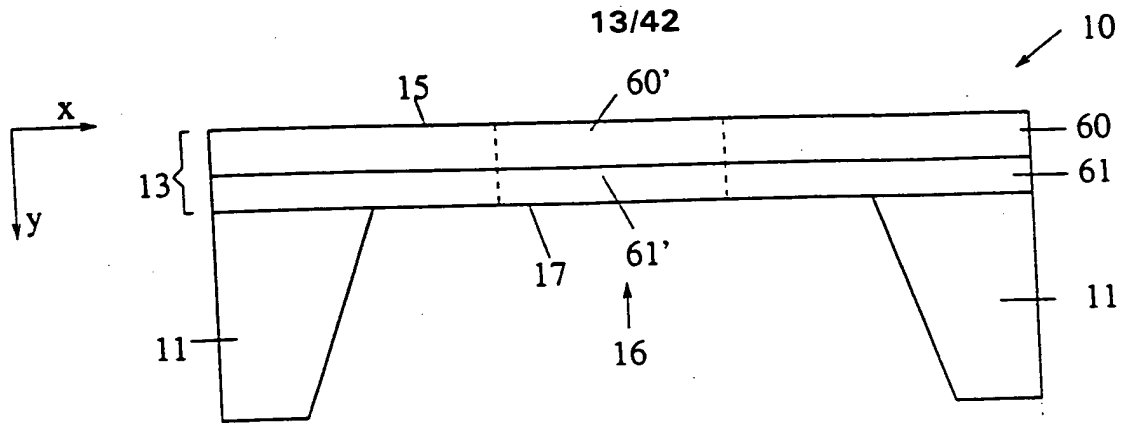


Figure 13a

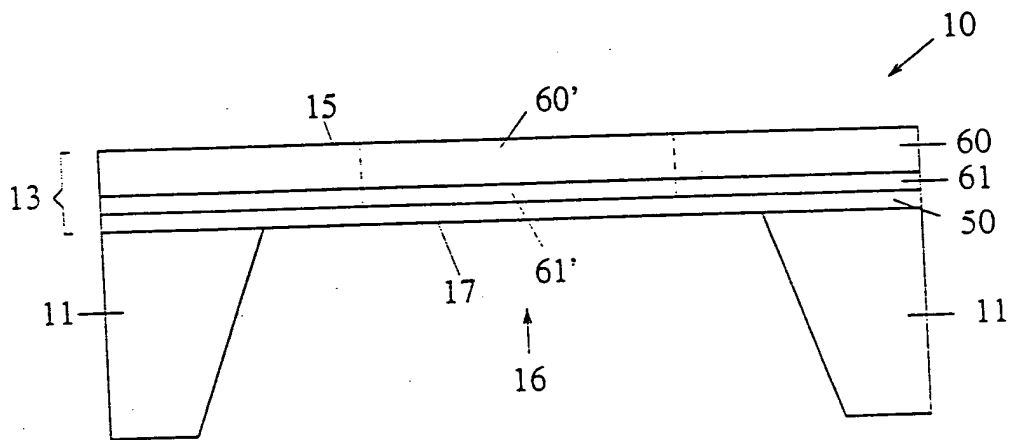


Figure 13b

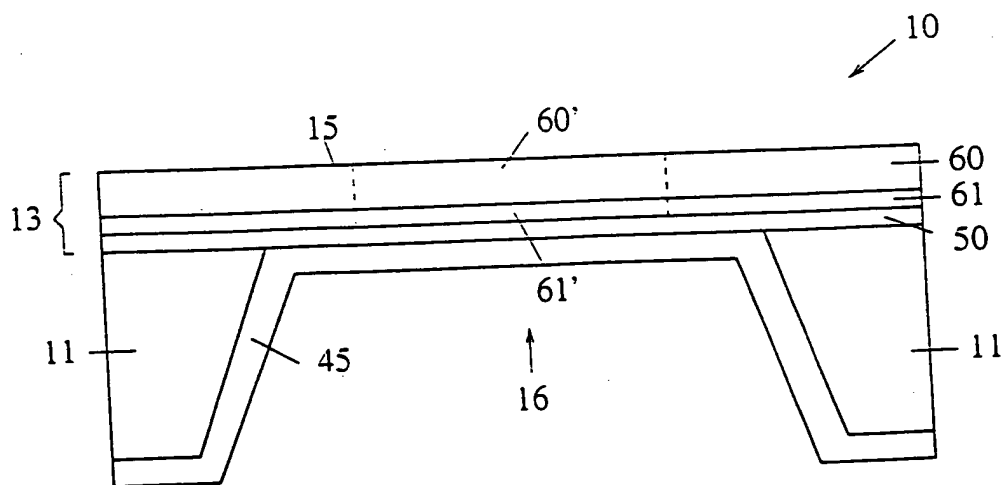


Figure 13c

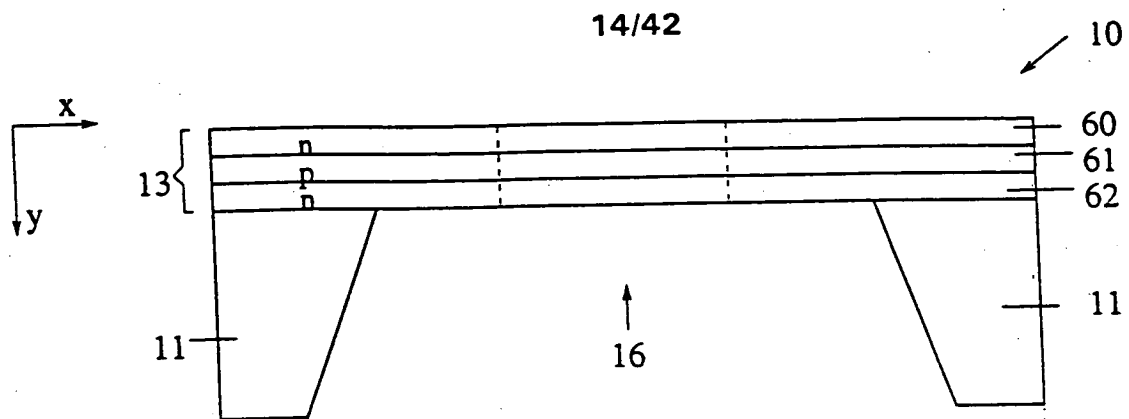


Figure 14a

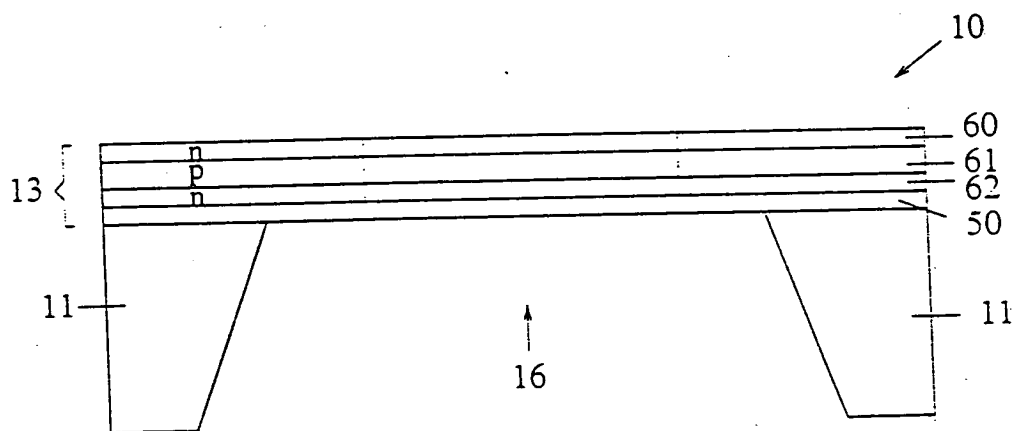


Figure 14b

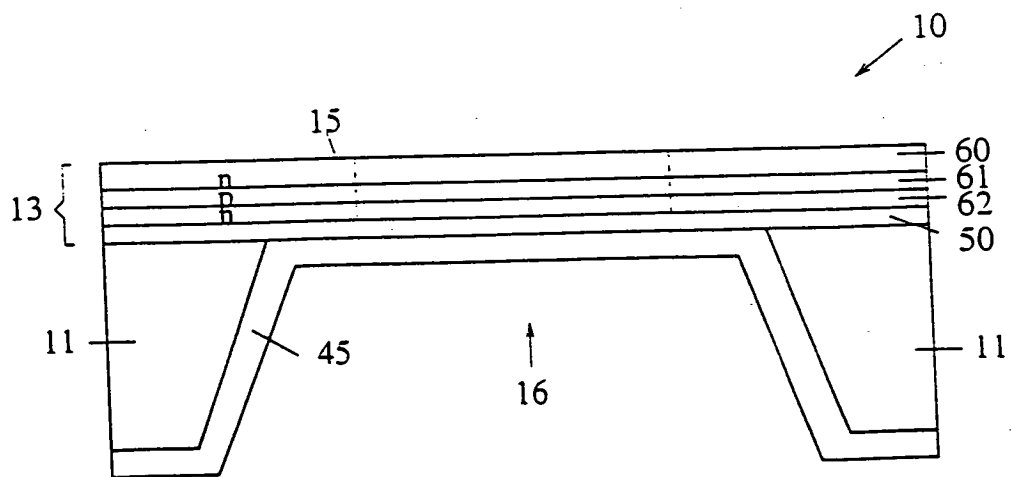


Figure 14c

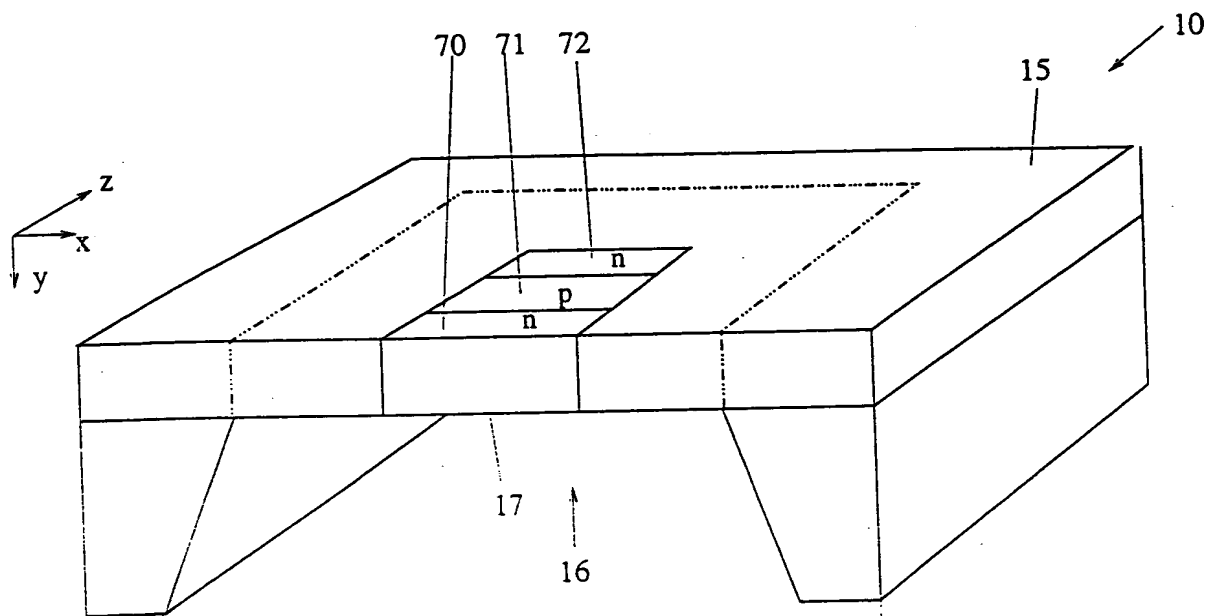


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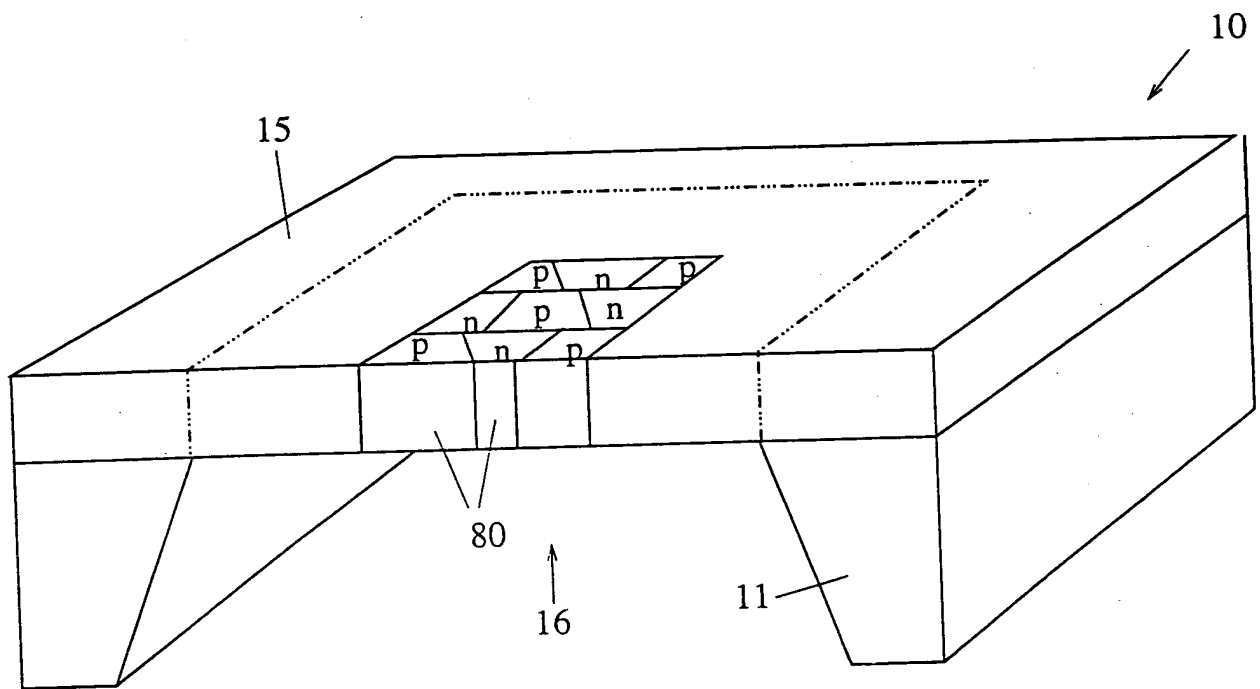


Figure 16

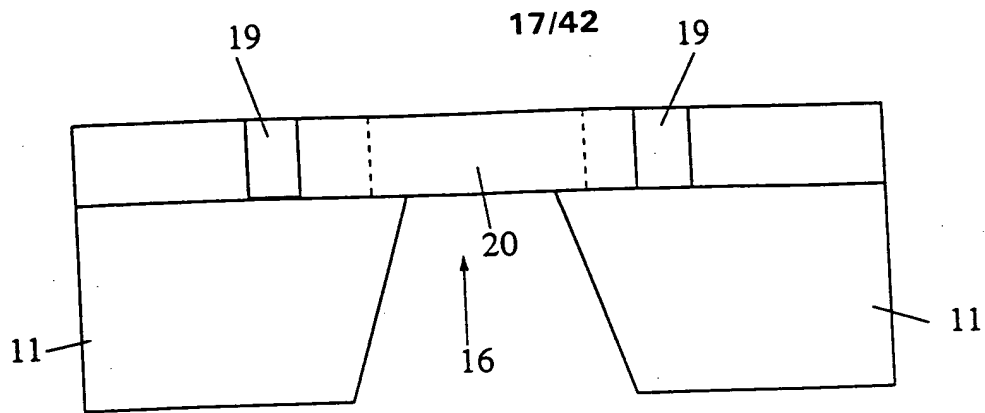


Figure 17a

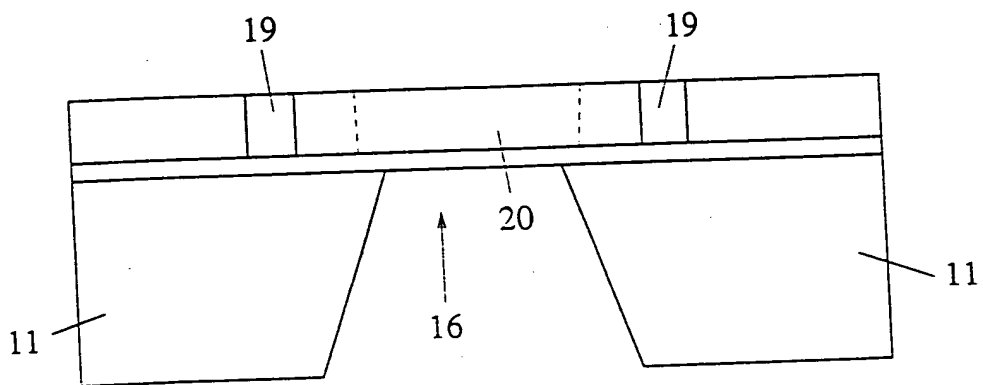


Figure 17b

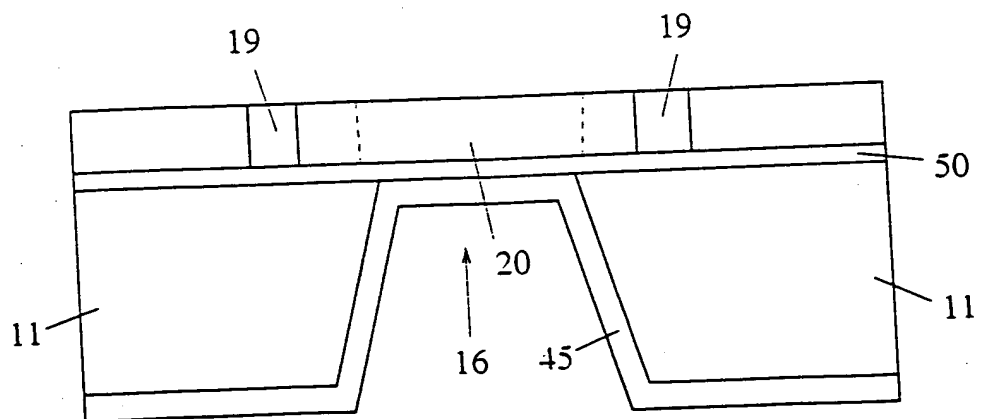


Figure 17c

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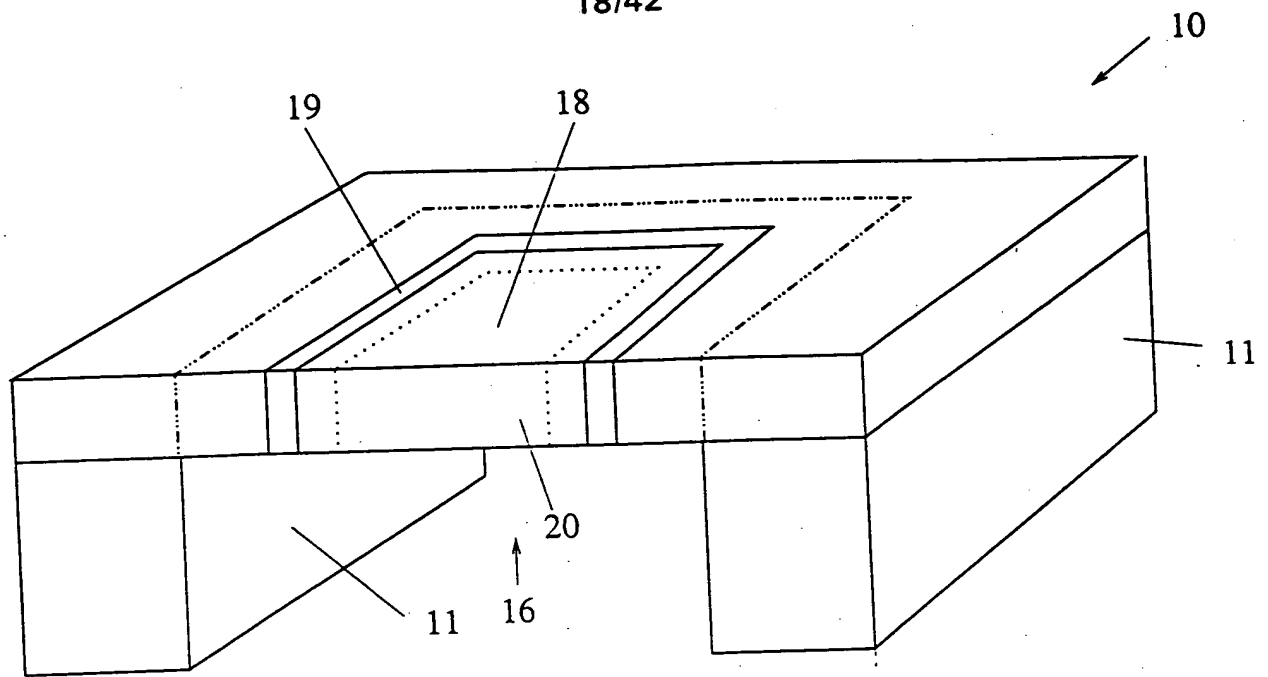


Figure 18a

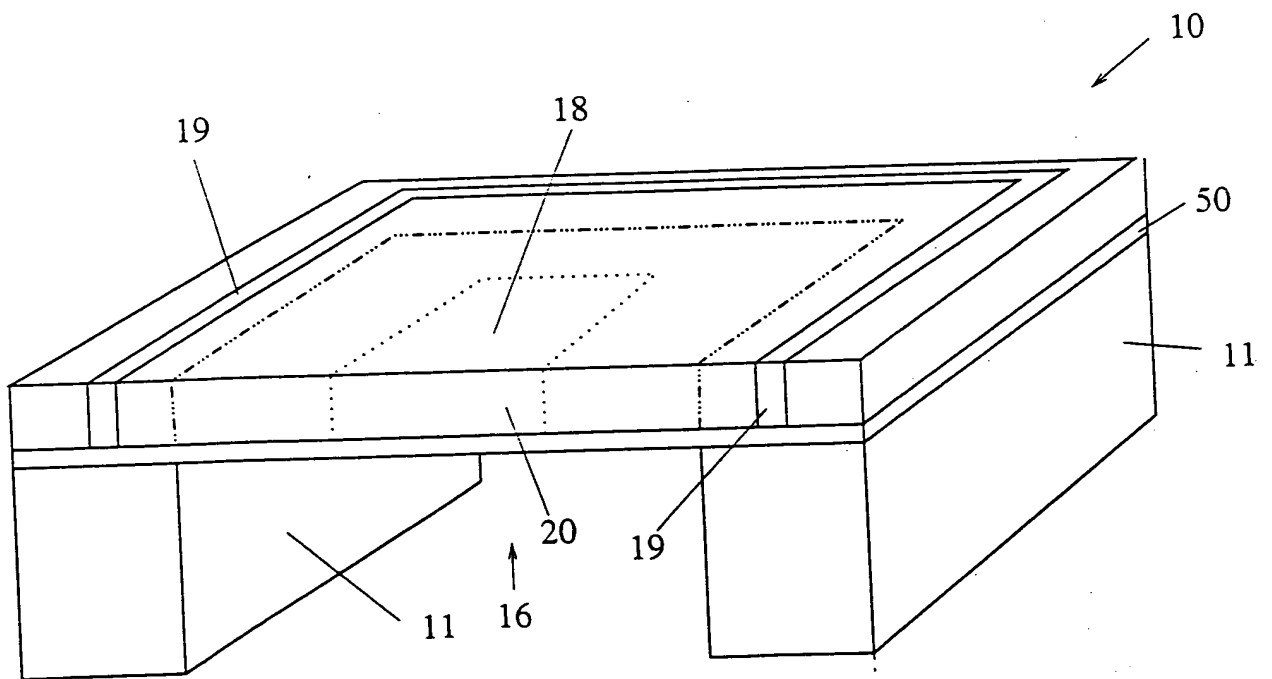


Figure 18b

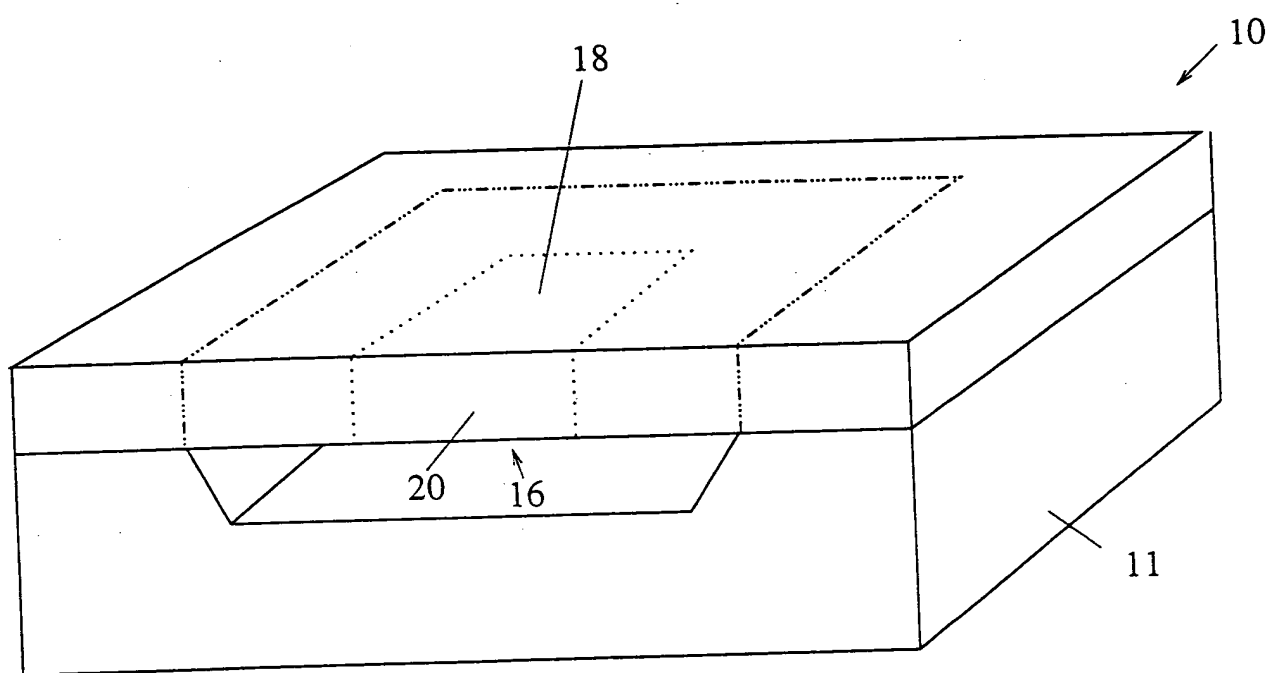


Figure 19

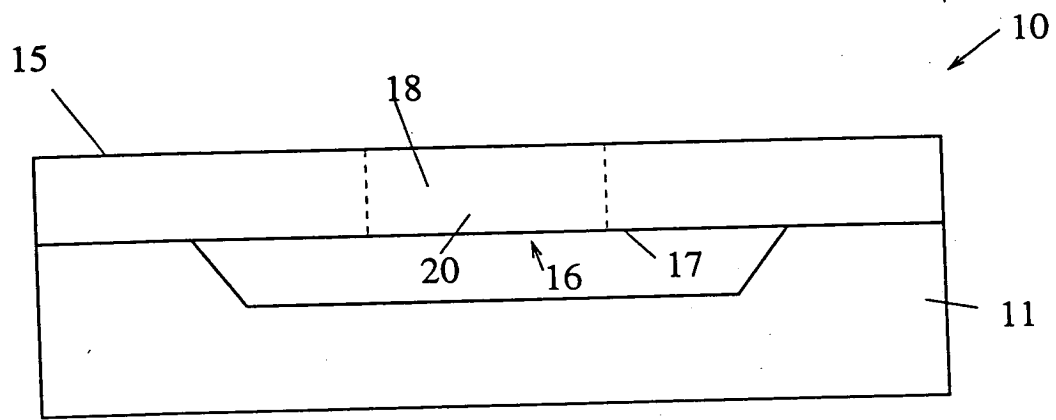


Figure 20

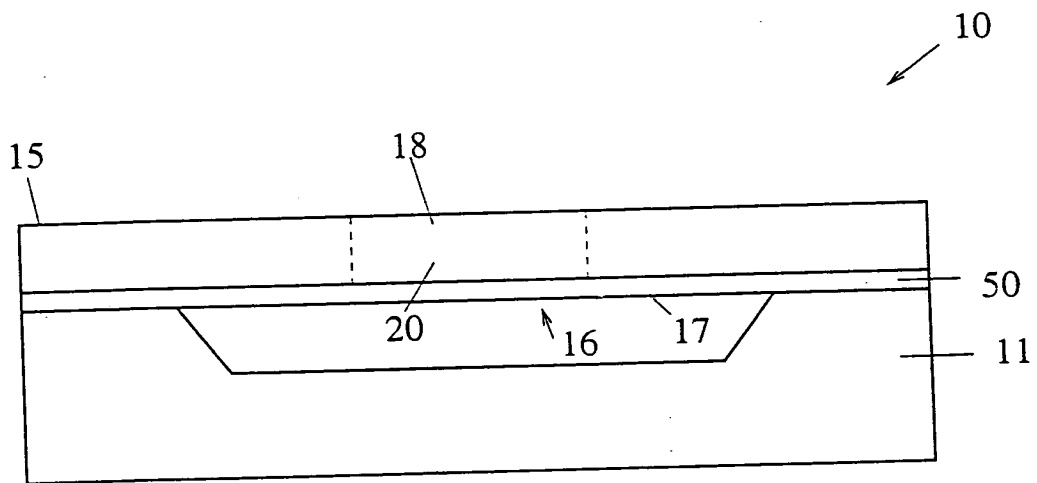


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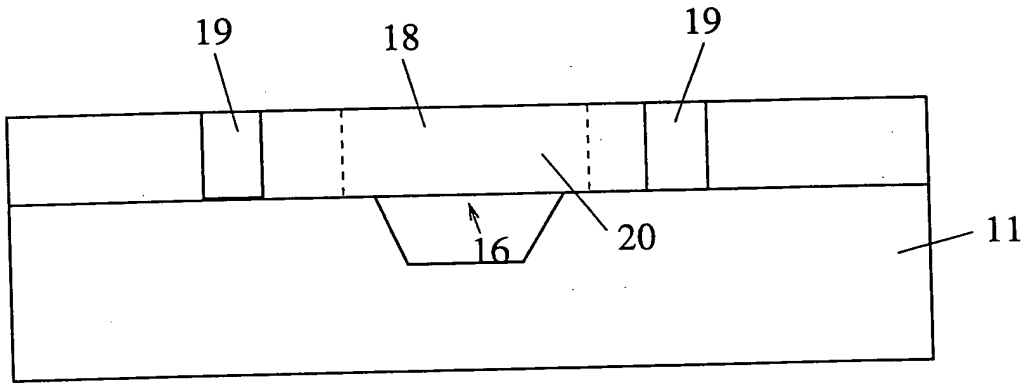


Figure 22a

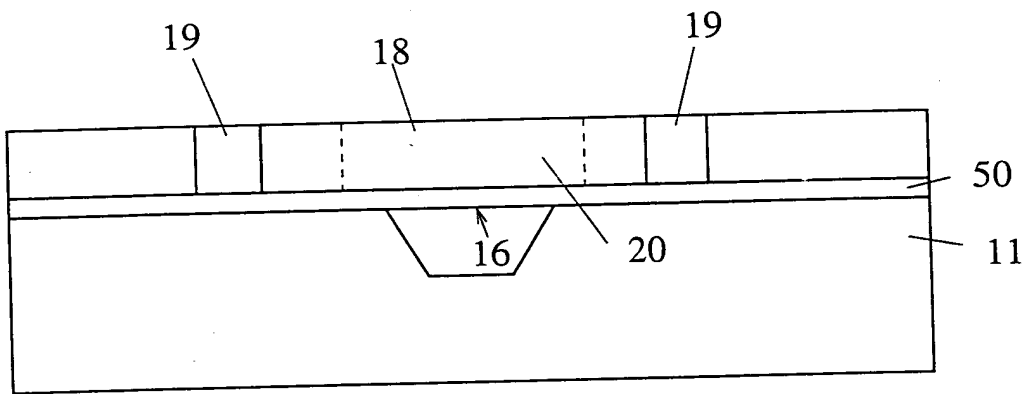


Figure 22b

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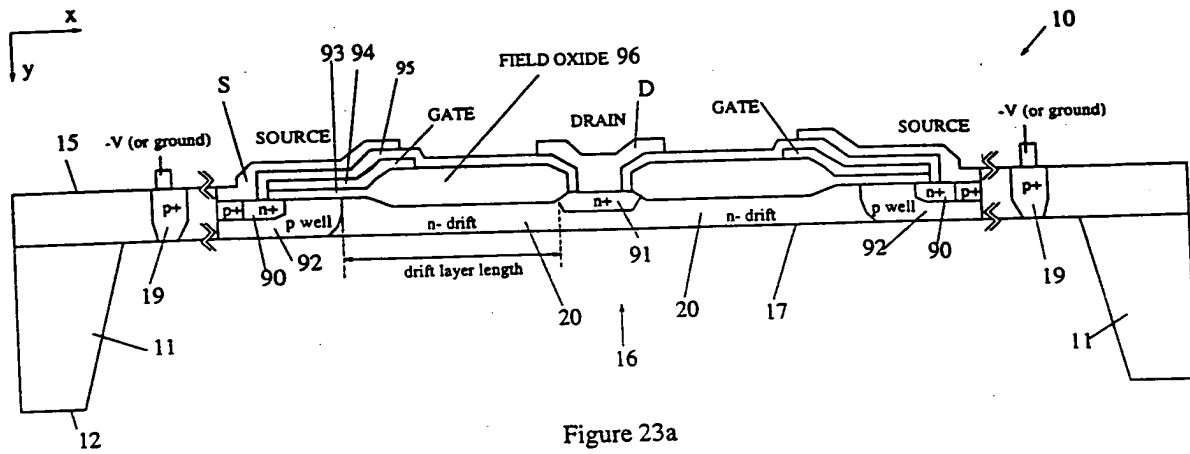


Figure 23a

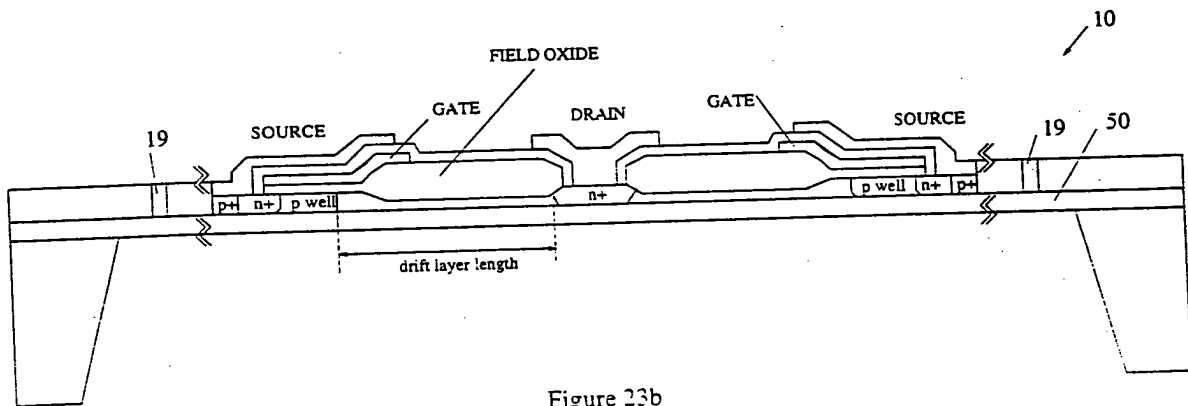


Figure 23b

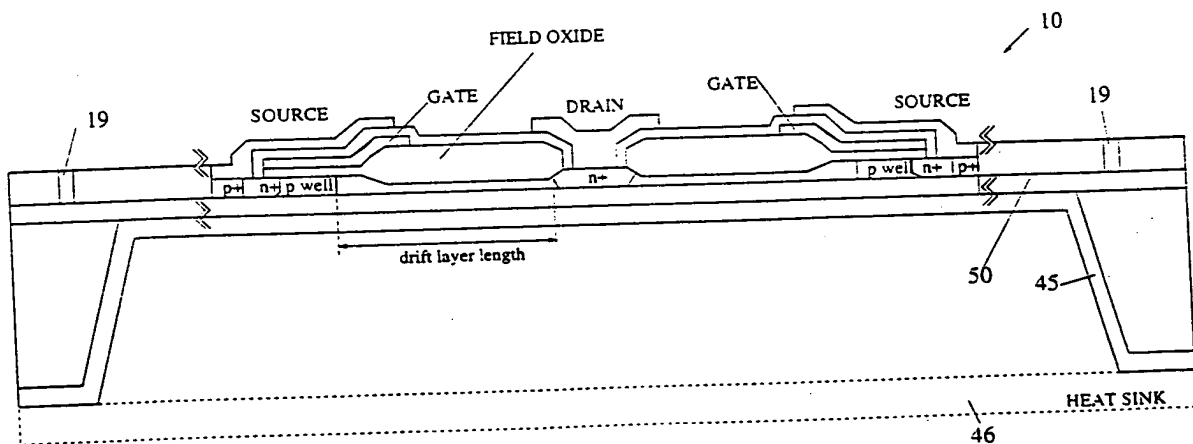


Figure 23c

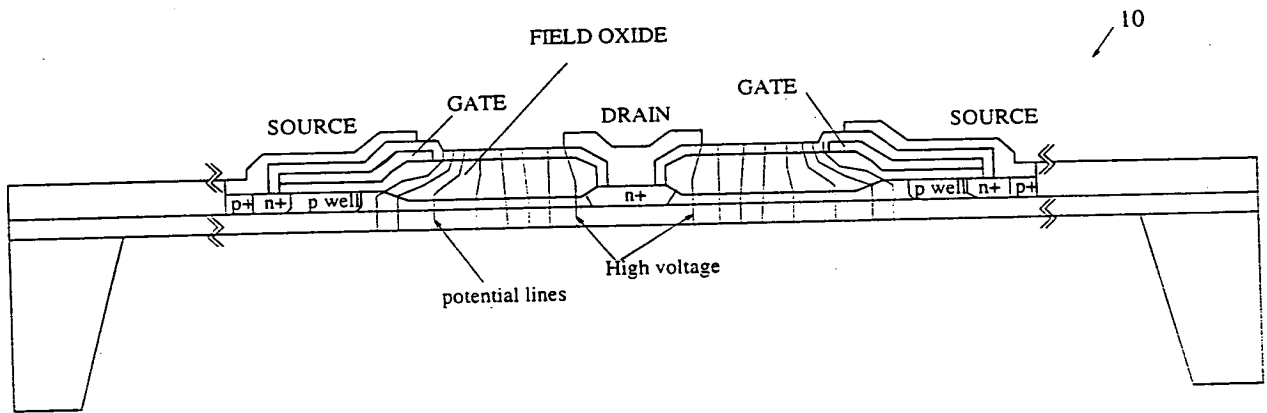


Figure 24

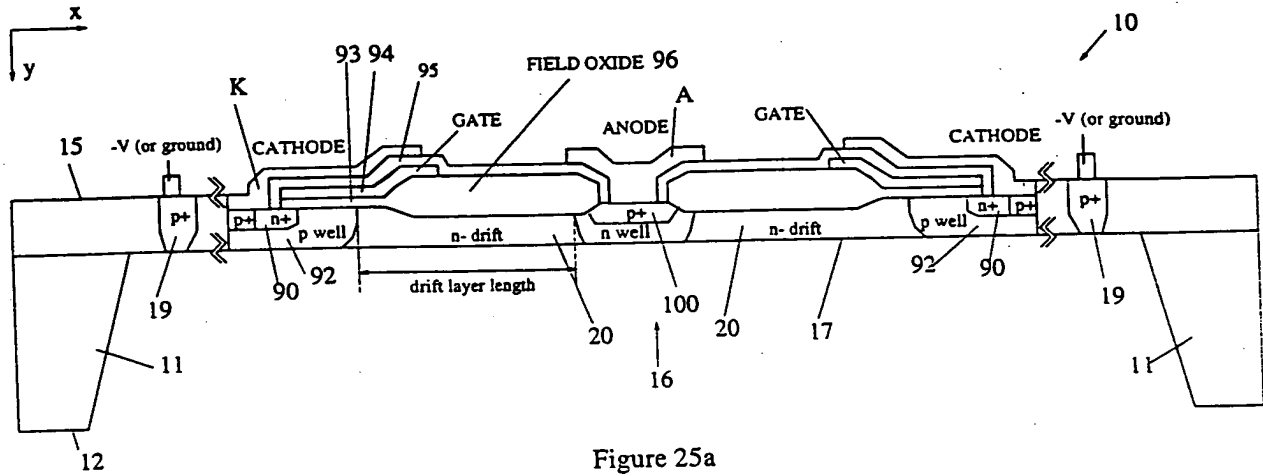


Figure 25a

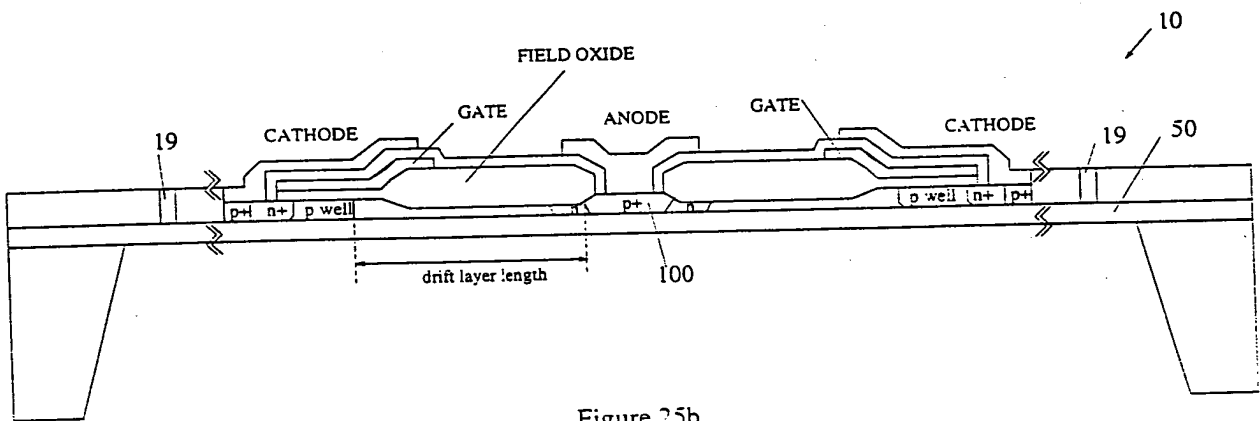


Figure 25b

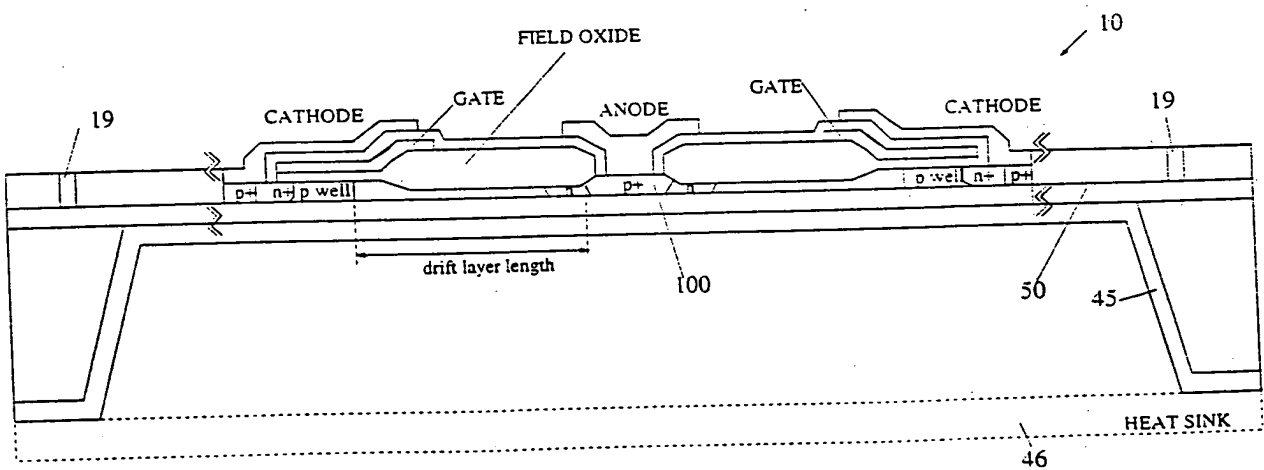


Figure 25c

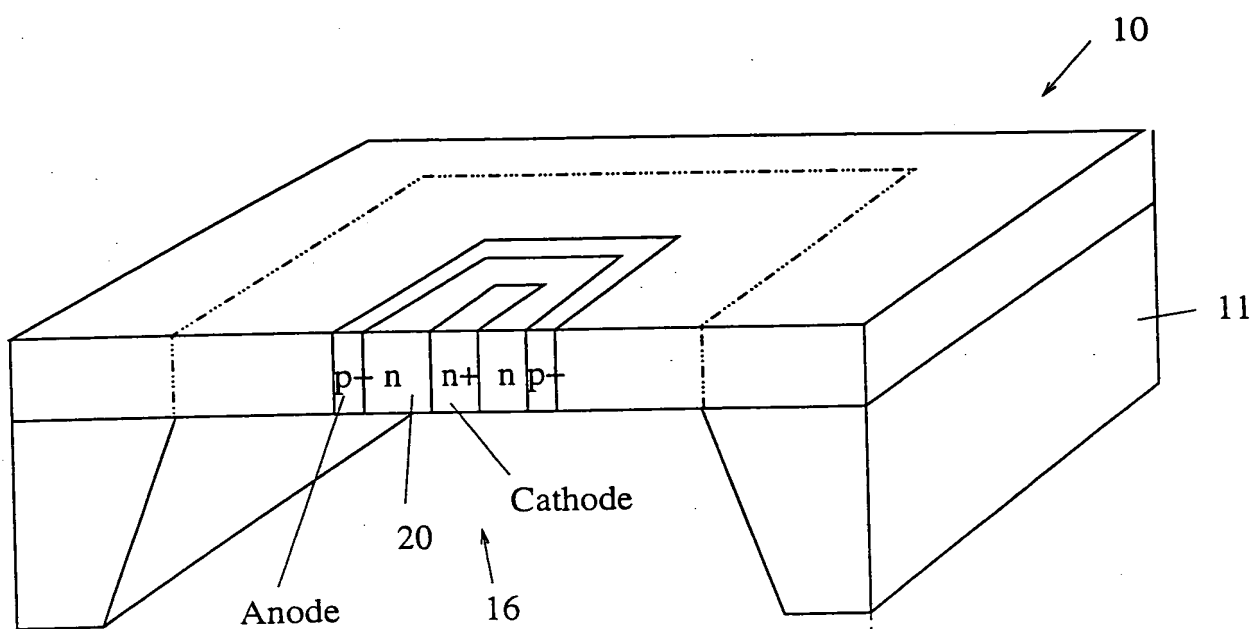


Figure 26a

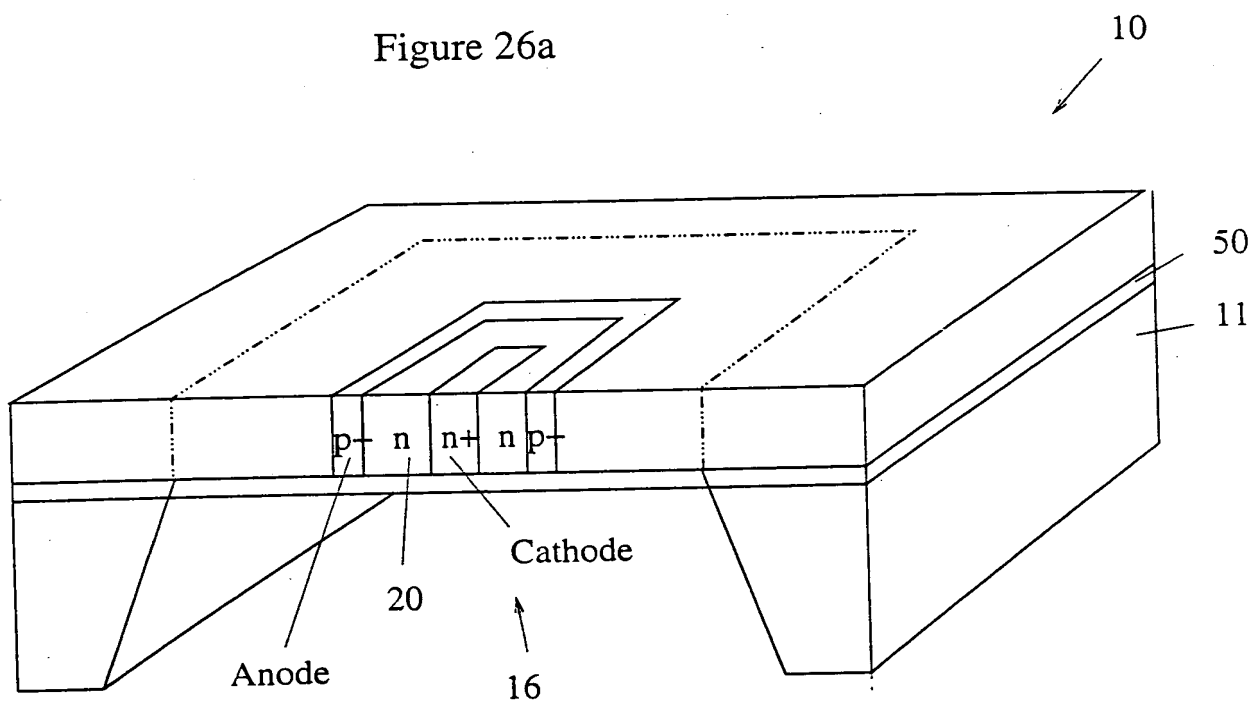


Figure 26b

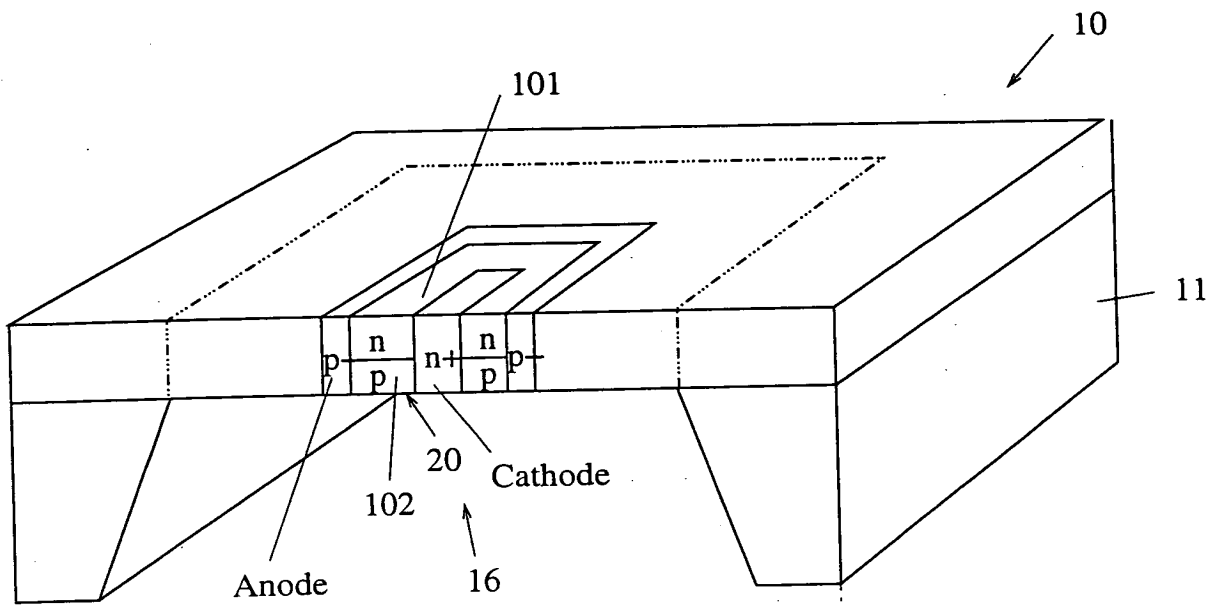


Figure 27a

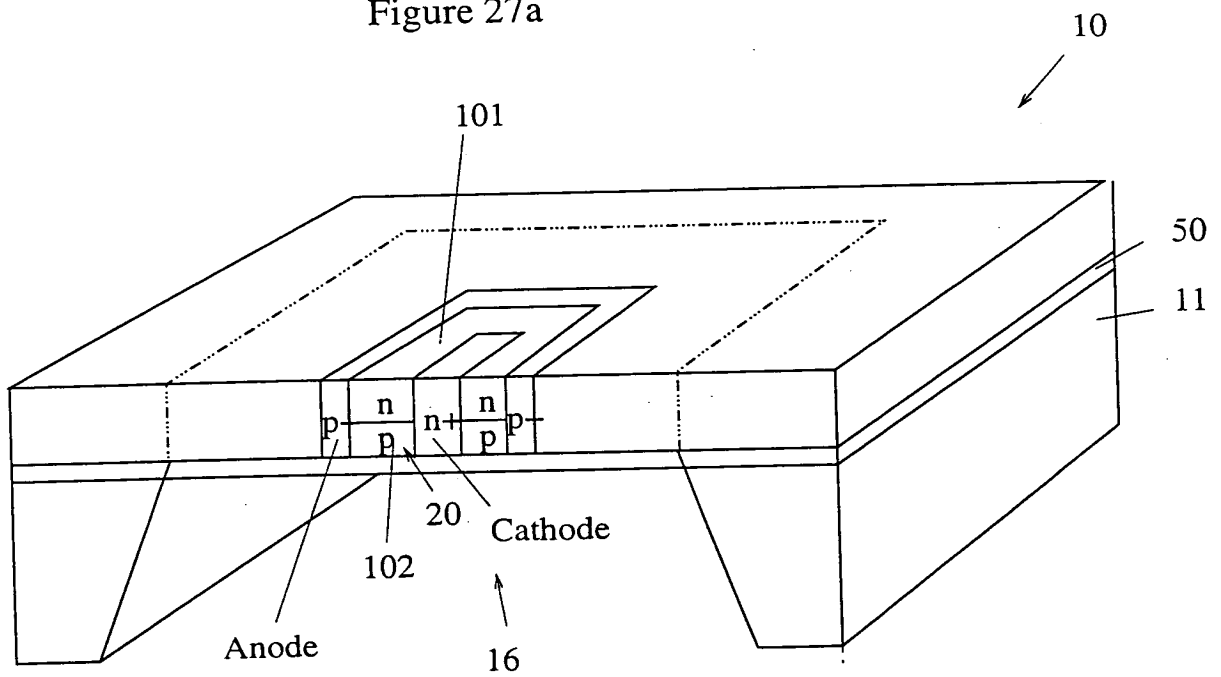


Figure 27b

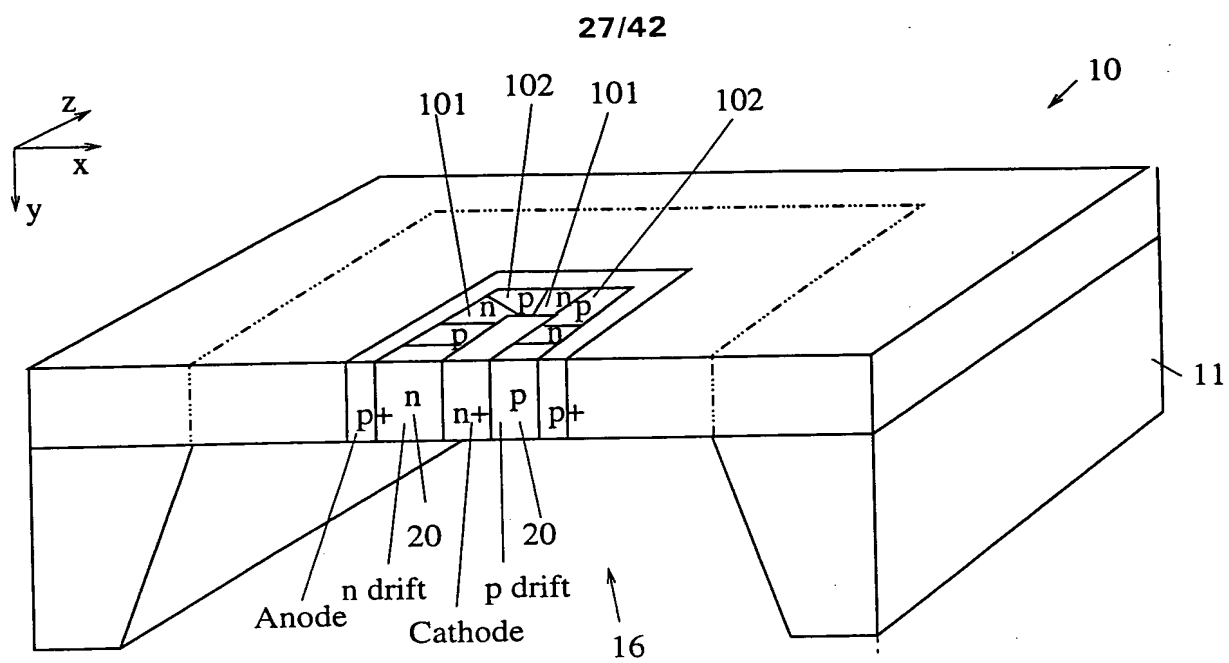


Figure 28a

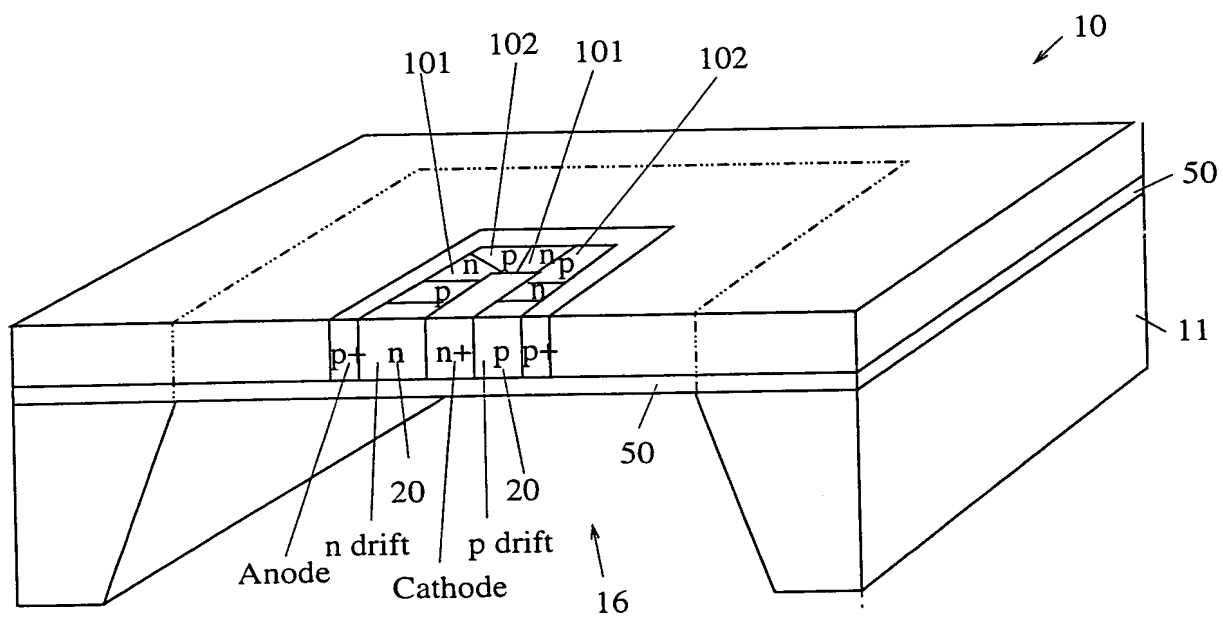


Figure 28b

Figure 29b

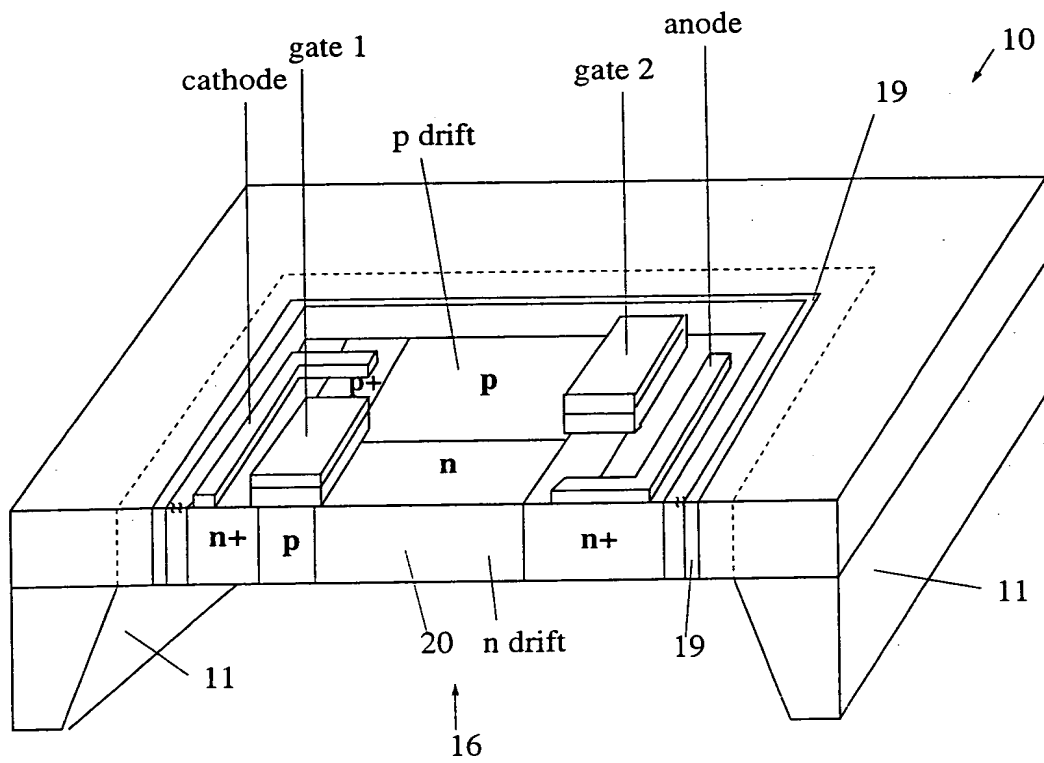


Figure 30

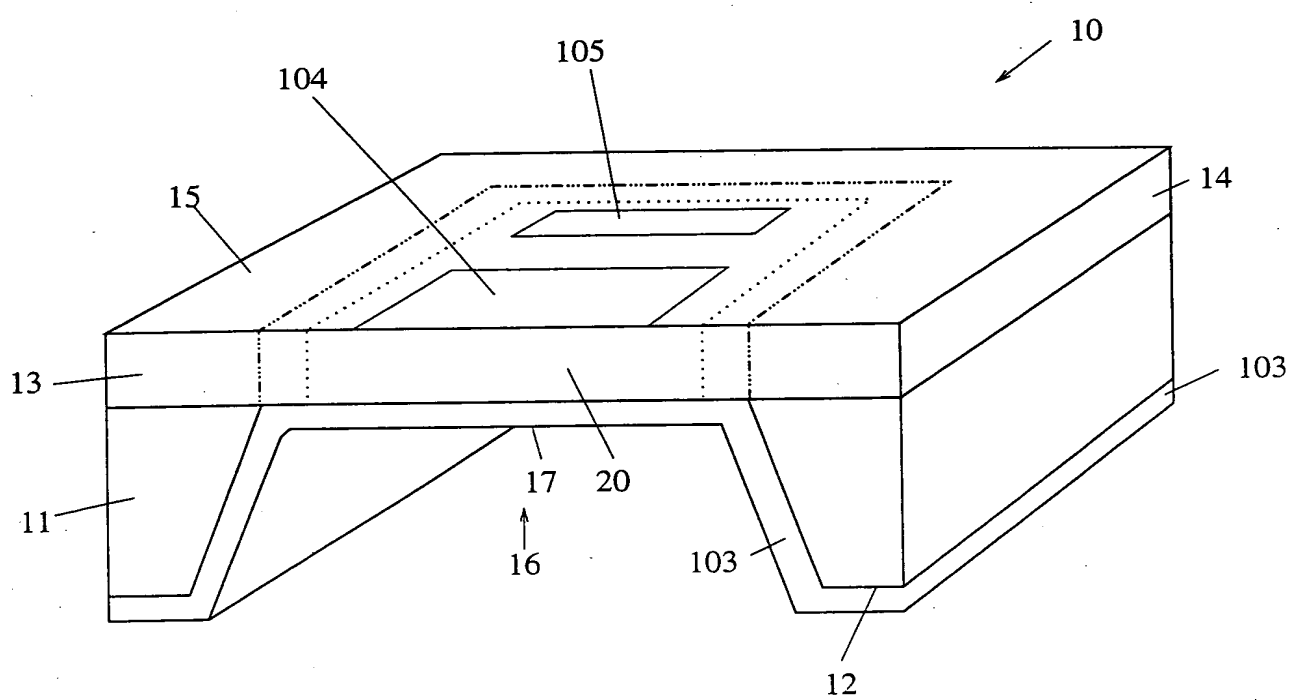


Figure 31

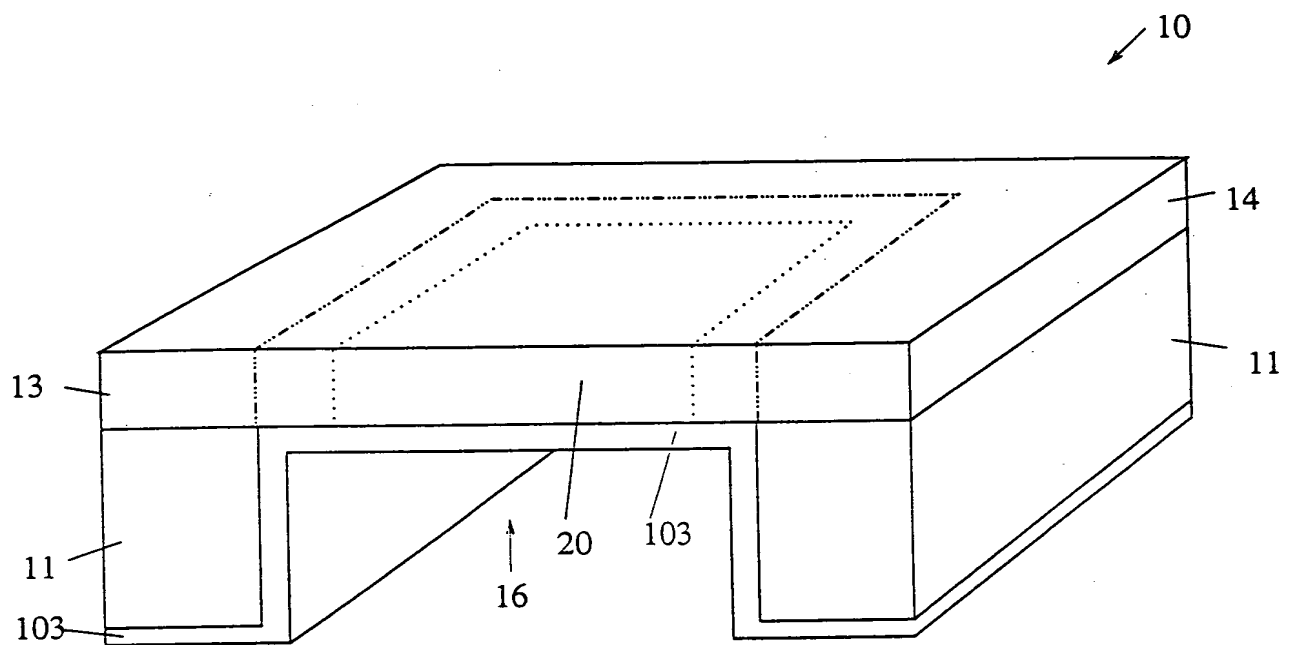


Figure 32

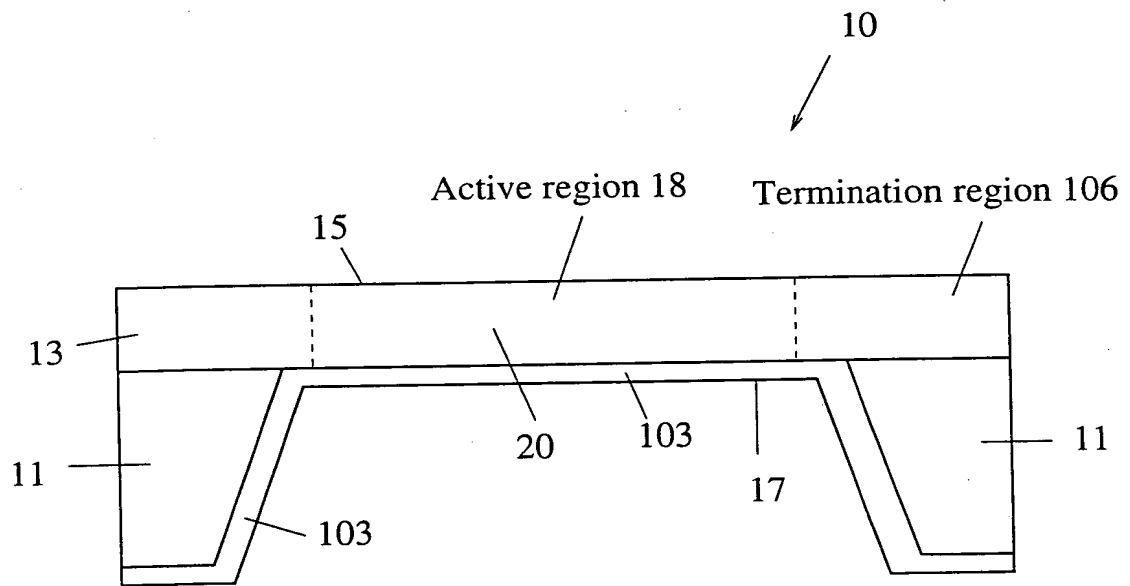


Figure 33

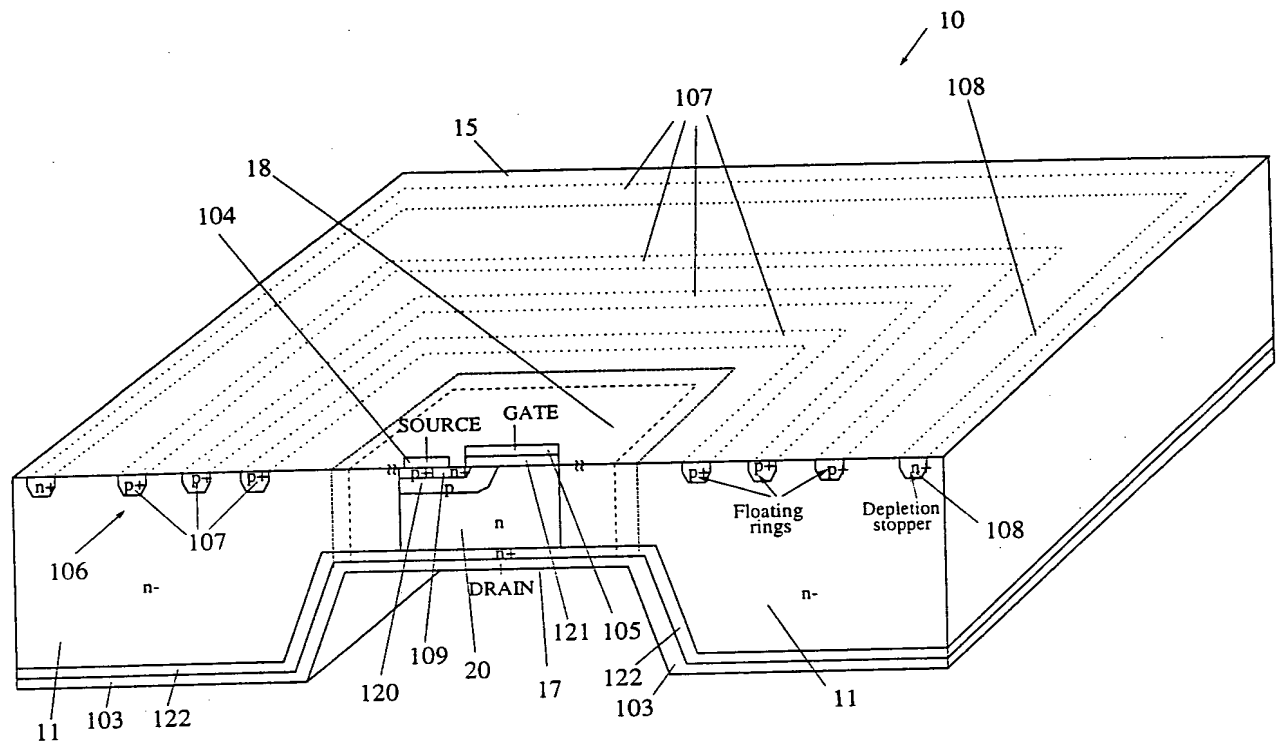


Figure 34

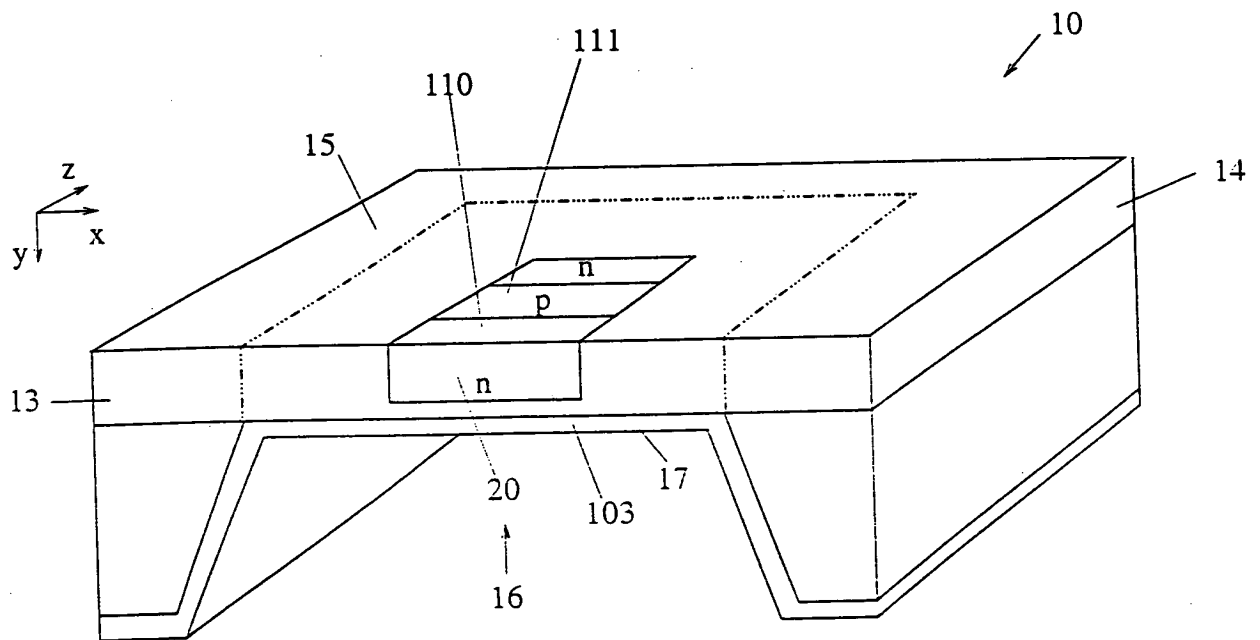


Figure 35

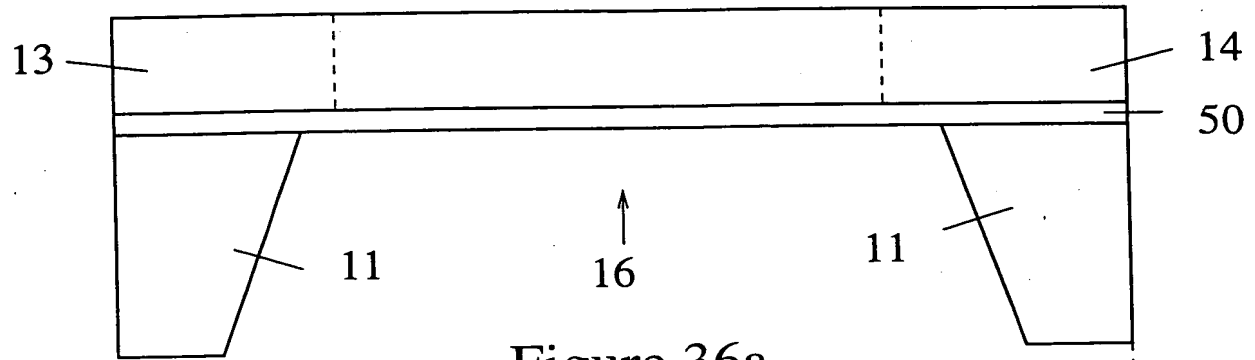


Figure 36a

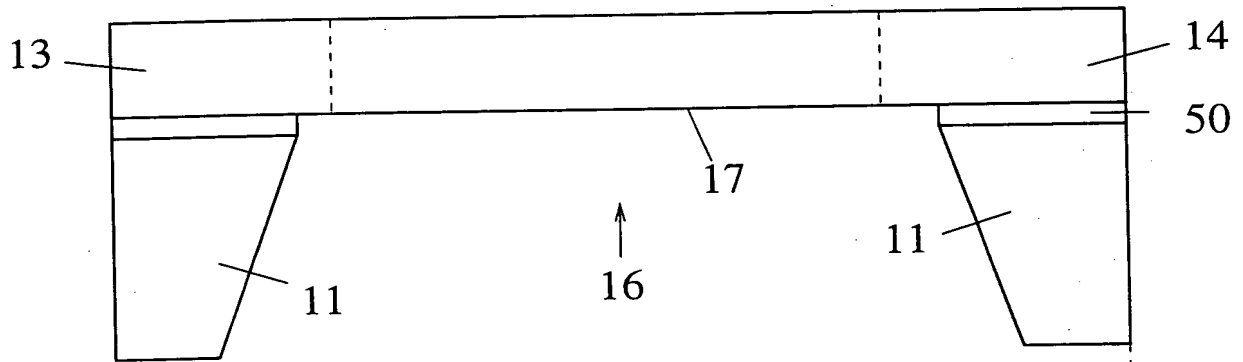


Figure 36b

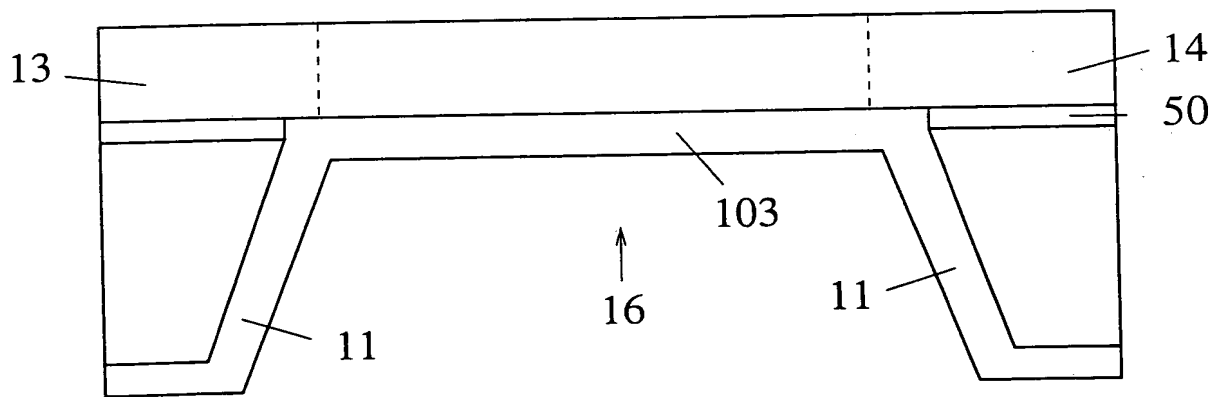


Figure 36c

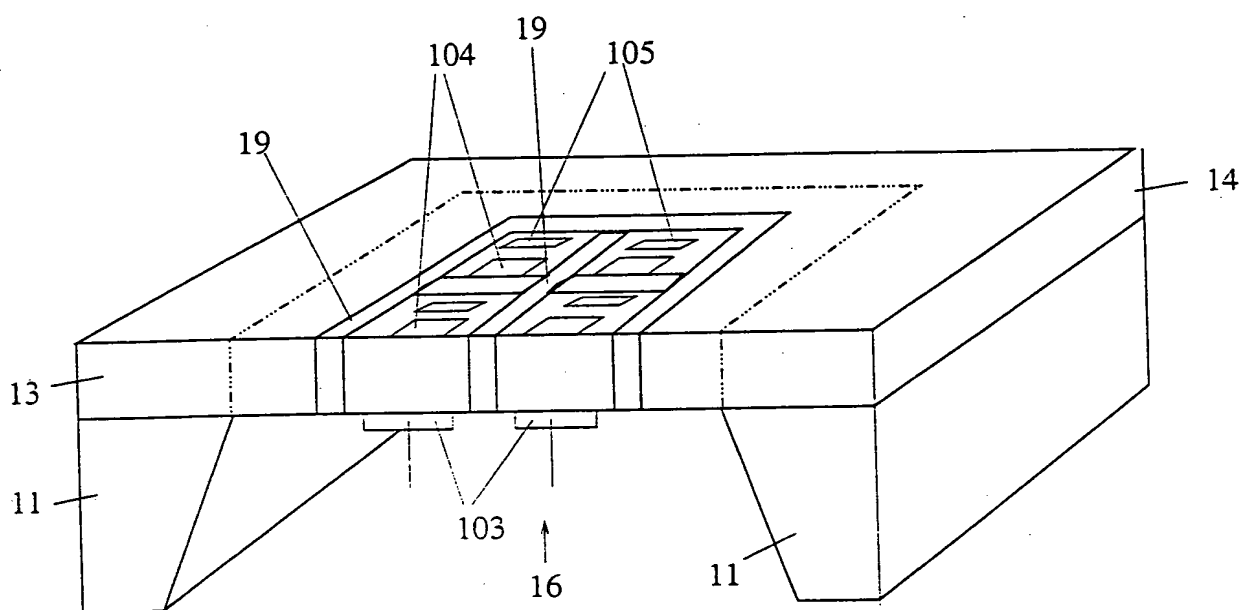


Figure 37

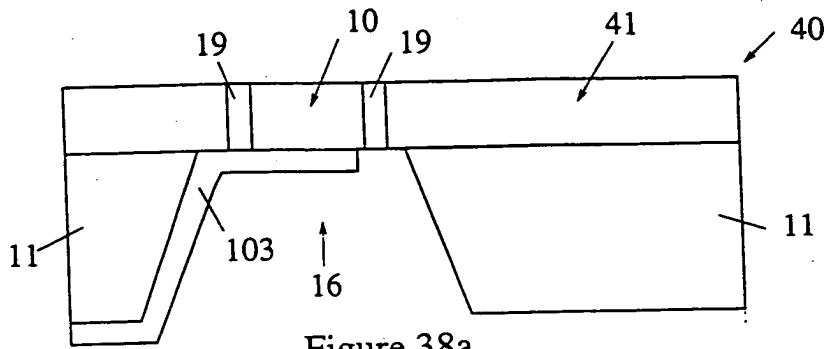


Figure 38a

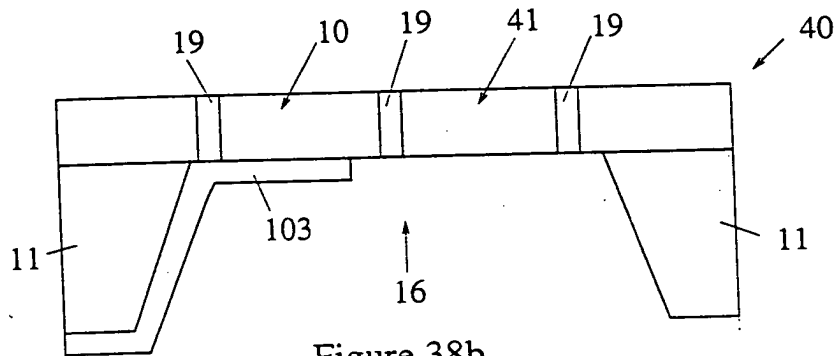


Figure 38b

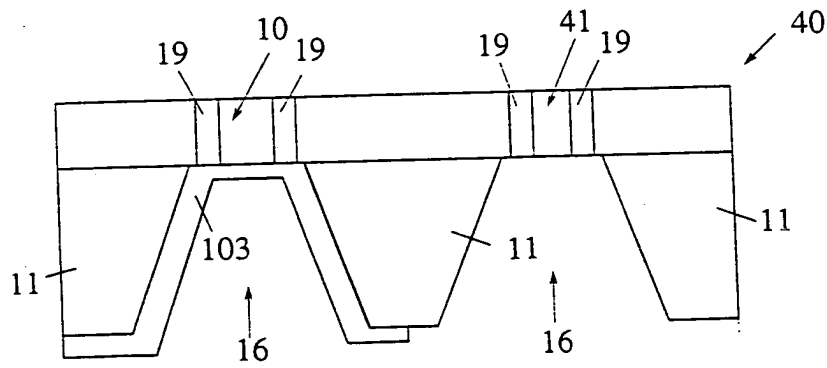


Figure 38c

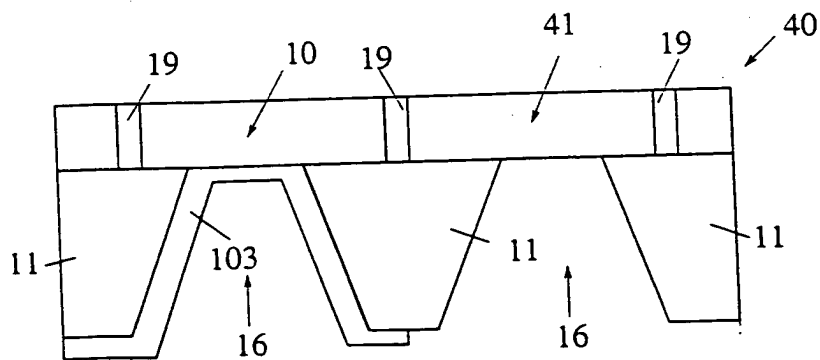


Figure 38d

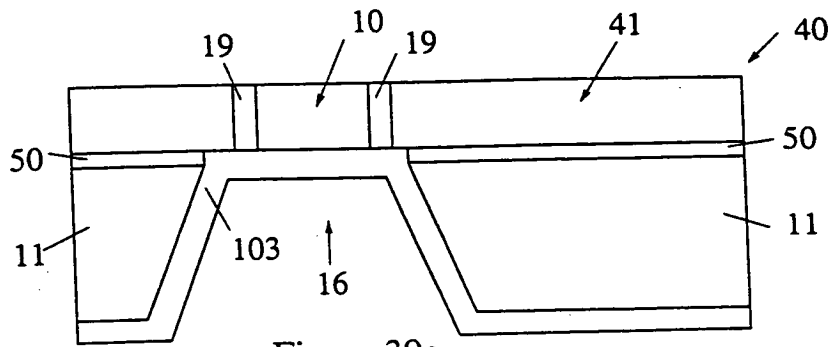


Figure 39a

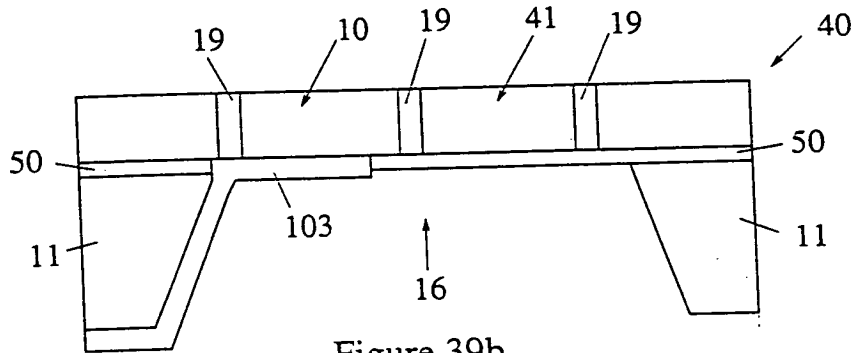


Figure 39b

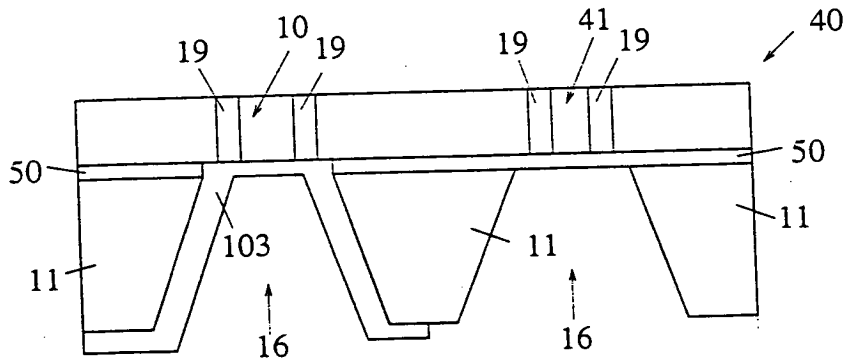


Figure 39c

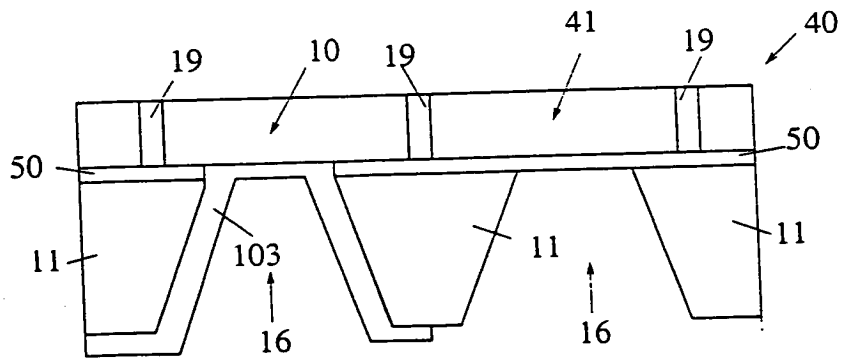
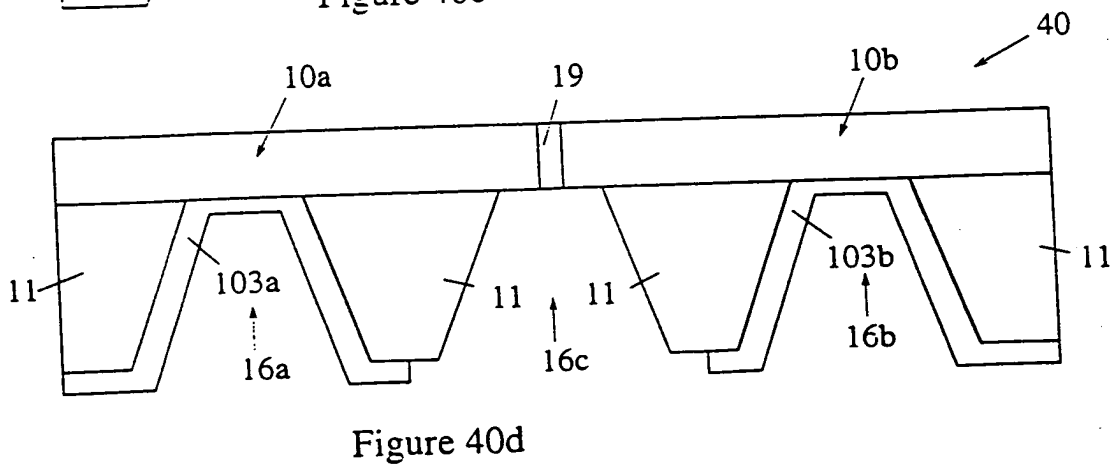
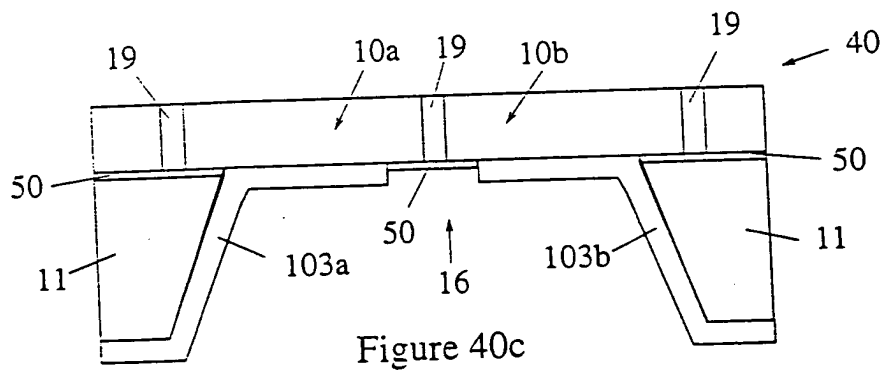
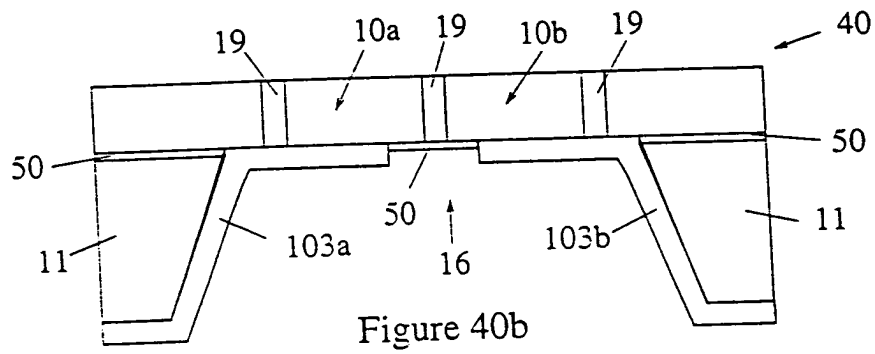
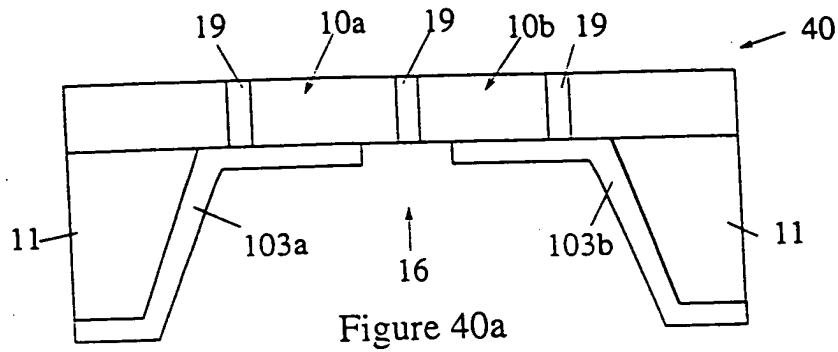


Figure 39d



[illegible][illegible]

A cross-sectional view of a semiconductor device. The device features a substrate with a top layer labeled '11'. A gate stack is formed on the substrate, consisting of a gate oxide layer (105) and a gate electrode (121). The gate electrode is connected to a 'GATE' terminal. A 'SOURCE' region is formed in the substrate, consisting of an n+ region (120) and a p+ region (122). A 'DRAIN' region is formed in the substrate, consisting of an n+ region (120) and a p+ region (122). The drain region is connected to a 'DRAIN' terminal (103). The device also includes a '16' region and a '15' region. The substrate is labeled '11'.

Figure 41c

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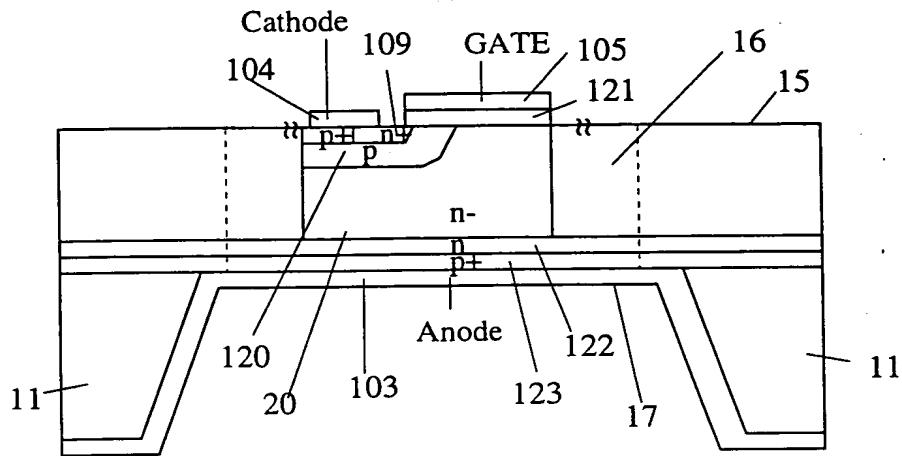


Figure 42a

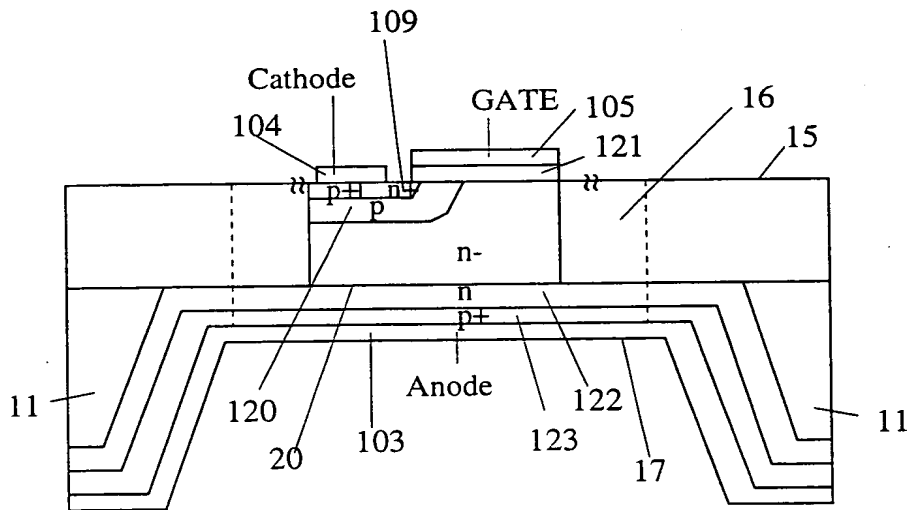


Figure 42b

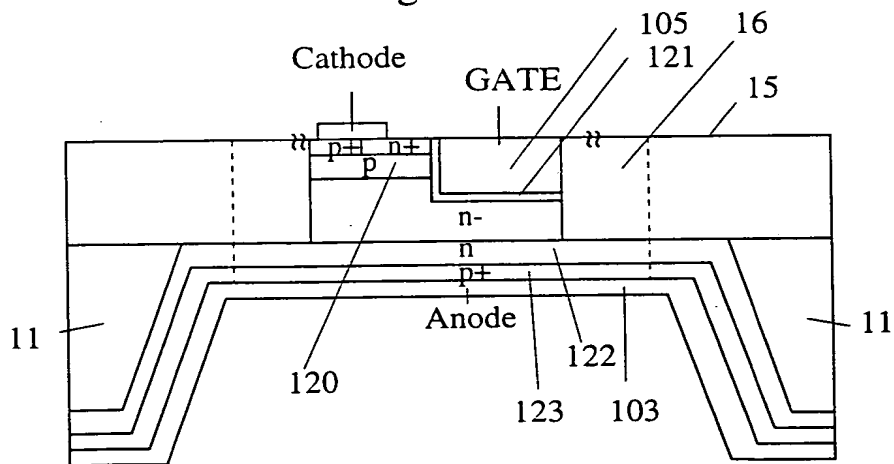


Figure 42c

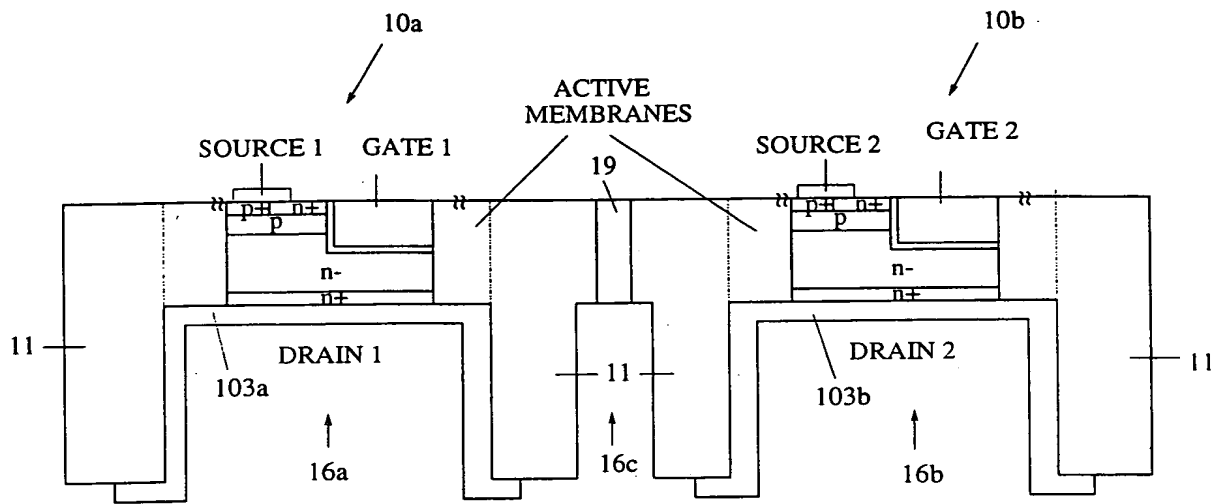


Figure 43a

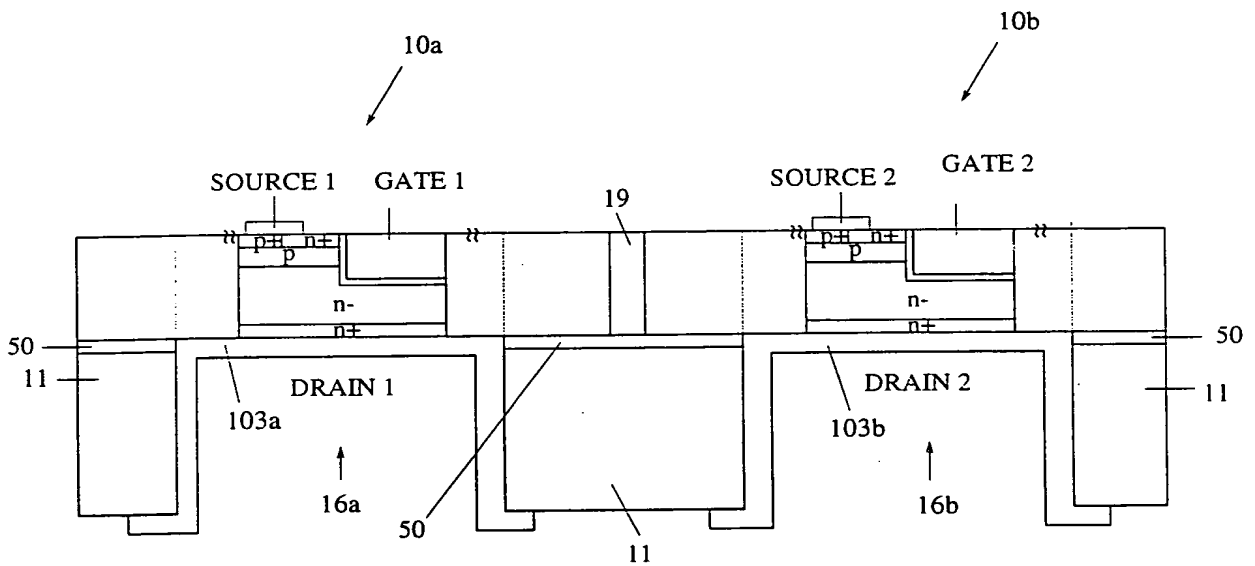


Figure 43b